iSBC® 308/309 MEMORY MANAGEMENT AND PROTECTION MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides user installation and operation information for the iSBC 308/309 Memory Management Multimodule Boards. These boards are intended to be used with Microsoft Corporation's Xenix® Operating System and other Unix®-like operating systems which require memory protection and mapping. This manual is *not* intended to be a tutorial on the subject of Memory Management.

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CONTENTS

PAGE

CHAPTER 1
GENERAL INFORMATION

1.1 Introduction 1-1
1.2 Description 1-1
1.3 Documentation & Equipment Supplied 1-2
1.4 Specifications 1-2

CHAPTER 2
INSTALLATION INSTRUCTIONS

2.1 Introduction 2-1
2.2 Board Dimensions & Mounting Clearances 2-1
2.3 Mounting Hardware 2-2
2.4 Installation Instructions 2-2
2.5 iSBC 308/309 Jumper Options 2-4
2.5.1 User Mode I/O Option 2-4
2.5.2 Number of Concurrent Processes Options 2-4

CHAPTER 3
PROGRAMMING INFORMATION

3.1 Introduction 3-1
3.2 Notation And Definitions 3-1
3.2.1 Logical Address 3-1
3.2.2 Physical Address 3-1
3.2.3 Page Concept 3-1
3.2.4 Process Concept 3-1
3.2.5 Trap Concept 3-2
3.2.6 Exceptions 3-2
3.2.7 System Request Flag 3-3
3.2.8 System/User Mode 3-3
3.2.9 iSBC 308/309 I/O Space 3-3
3.3 Commands 3-4
3.3.1 Map Memory Command (System Mode Only) 3-4
3.3.2 Set Process Register Commands (System Mode 3-5
3.3.3 System Call Command (System/User Mode) 3-5
3.3.4 Clear Status Command (System/User Mode) 3-6
3.3.5 Set/Clear System Mode Command (System/User) 3-6
3.4 System Software Considerations 3-6
3.4.1 Initialization 3-7
3.4.2 Process Switching 3-9
3.4.3 Trap Handlers 3-10
3.4.3.1 Exceptions 3-10
3.4.3.2 8086 Architecture Considerations 3-12
3.4.3.3 System Calls 3-12
3.4.3.4 Interrupts 3-12

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 Introduction 4-1
4.2 General Description 4-1

CONTENTS (CONT.)

4.3 Functional Description 4-1
4.3.1 System Interface 4-2
4.3.2 Timing Logic 4-2
4.3.3 I/O Decoder 4-4
4.3.4 Mode Control 4-5
4.3.5 Exception Logic 4-6
4.3.6 Process Register and Memory Map 4-6
4.3.7 Interface Control 4-7

CHAPTER 5
SERVICE INFORMATION

5.1 Introduction 5-1
5.2 Service And Repair Assistance 5-1
5.3 Replacement Parts 5-2
5.4 Schematic Diagrams 5-2

ILLUSTRATIONS

FIGURE	TITLE	PAGE
1-1.	iSBC 308/309 Memory Management Boards	1-1
2-1.	iSBC 308/309 Physical Dimensions (Inches)	2-1
2-2.	iSBC 308/309 Mounting Clearances	2-2
2-3.	iSBC 308/309 Mounting Technique	2-3
2-4.	iSBC 309 Board on iSBC 88/30 Board	2-3
3-1.	Logical Page Notation	3-2
3-2.	iSBC 308/309 User & System I/O Space	3-3
3-3.	Example Memory Map	3-7
3-4.	Typical Initialization	3-8
3-5.	Typical Memory Mapping Routine	3-9
3-6.	Typical Procedure For Activating A User Process	3-10
3-7.	Typical User Mode To System Mode Process	3-11
4-1.	Host - iSBC 308/309 Interface Timing	4-1
5-1.	iSBC 308 Board	5-4
5-2.	iSBC 309 Board	5-5
5-3.	iSBC 308 Schematic Diagram	5-6
5-4.	iSBC 309 Schematic Diagram	5-10

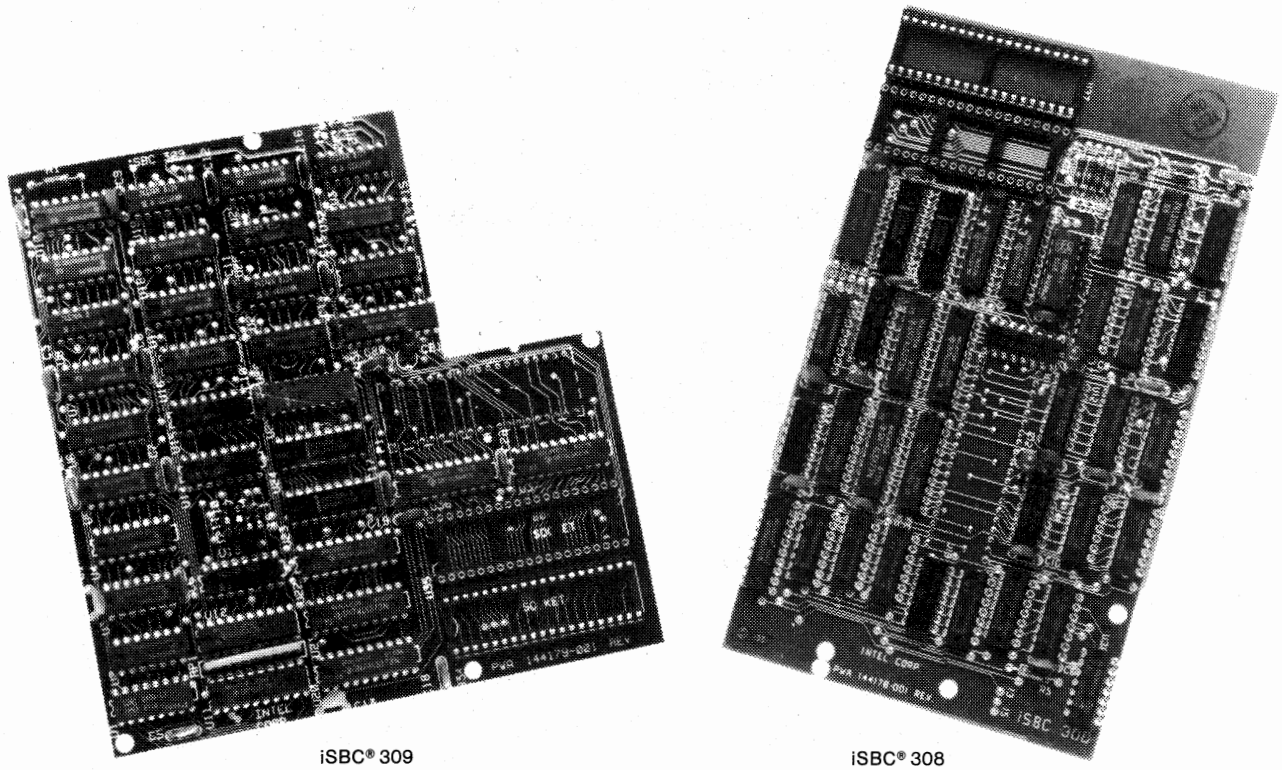
TABLES

TABLE	TITLE	PAGE
2-1.	Process Selection Jumpers	2-4
2-2.	Process Register Format	2-4
4-1.	iSBC 308/309 AC Characteristics	4-2
4-2.	iSBC 308/309 DC Characteristics	4-3
4-3.	Decode Prom Map	4-4
5-1.	iSBC 308 Board Parts List	5-2
5-1.	iSBC 309 Board Parts List	5-3

1.1 INTRODUCTION

The iSBC 308 and iSBC 309 Memory Management Multimodule boards are designed to add operating system memory management capability to the Intel 16-bit, 8086-based family of single board computers (Figure 1-1). The iSBC 308 board can be installed only on the iSBC 86/12A Single Board Computer. The iSBC 309 board is compatible with the iSBC 86/14 board and the iSBC 86/30 board. The iSBC 308/309 boards each plug directly into the processor socket of the host board, and do not require any other interface. Power is supplied by the host board.

When installed, the iSBC 308 board prevents use of any Multimodule boards on the iSBC 86/12A board. The iSBC 309 prevents the use of one iSBX Multimodule connector, but permits the use of Multimodule expansion boards and the second iSBX connector. The iSBC 309 board allows 5 MHz or 8MHz processing.



iSBC® 309 iSBC® 308

Figure 1-1. iSBC® 308/309 Memory Management Boards

1.2 DESCRIPTION

The iSBC 308/309 boards each provide two modes of 8086 operation: a system (or priviledged) mode and a user mode. In the system mode the operating system can map the logical address space of a user mode process anywhere in the 8086 1-megabyte physical address space. Logical memory is mapped in 2K byte blocks (pages). Each page can be marked as non-existent, read only, or read/write memory.

In the user mode, a process cannot alter the memory map or change the process number (refer to Section 3.2.4). Depending on the configuration, up to 31 user process maps (plus one system process) with independent memory maps can be mapped at once. The ability to support multiple processes reduces the operating system overhead by reducing the time spent loading the memory map.

Each user mode process is restricted to its own address space as defined by the operating system. Invalid memory references cause control to be transferred back to the operating system. The following chart illustrates the relationship between processes, pages and memory size.

Number of Process Maps	Number of Pages Per Process	Memory Size Per Process (Bytes)
2	512	1 Megabyte
4	256	512K
8*	128*	256K*
16	64	128K
32	32	64K

Note: * = Xenix® compatible configuration.

1.3 DOCUMENTATION AND EQUIPMENT SUPPLIED

The iSBC 308/309 boards are each shipped with a set of schematic diagrams and all the necessary hardware for installation onto the host board. The schematic diagrams should be kept for future reference. These diagrams may be more recent than the diagrams in this manual.

1.4 SPECIFICATIONS

Power Requirements:	+5 VDC ±5% @ 2.00 Amps Maximum
Operating Temperature Range:	0°C - 55°C (32°F - 131°F)
Maximum Humidity:	90% non-condensing
Physical Dimensions:	Refer to Figure 2-1.
Weight (without 8086/8087):	140 grams (5 oz)

CHAPTER 2
INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

The iSBC 308 board can be installed only on the iSBC 86/12A Single Board Computer. The iSBC 309 board is compatible with the iSBC 86/14 board and the iSBC 86/30 board. This chapter provides instructions for installing the iSBC 308/309 boards on their respective host boards.

2.2 BOARD DIMENSIONS AND MOUNTING CLEARANCES

Figure 2-1 gives the pertinent physical dimensions for the iSBC 308 board and the iSBC 309 board. Figure 2-2 shows the mounting height clearances.

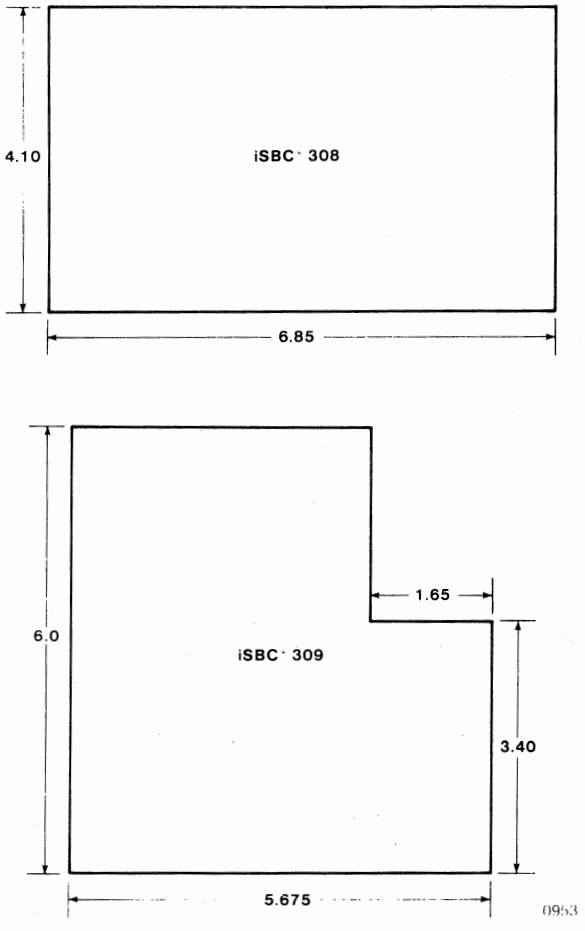


Figure 2-1. iSBC® 308/309 Physical Dimensions (Inches)

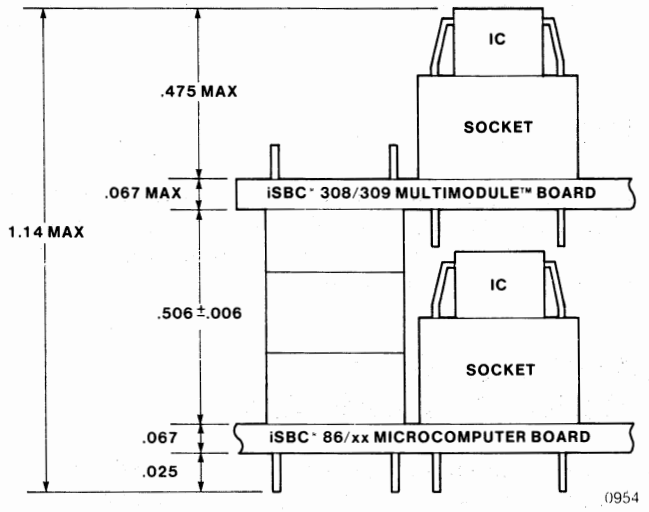


Figure 2-2. iSBC® 308/309 Mounting Clearances

2.3 MOUNTING HARDWARE

The following hardware is shipped with the iSBC 308/309 boards:

a. Two 1/4 inch X 1/2 inch threaded, non-conductive spacers; and
b. Four 1/4 inch nylon roundhead screws.

2.4 INSTALLATION INSTRUCTIONS

The following steps outline iSBC 308/309 installation:

a. Remove host board from system. If removing host board from an active system, turn all power off first.

b. For the iSBC 308 board, remove all host Multimodule expansion boards.

c. For the iSBC 309 board, remove leftmost iSBX Multimodule board, if present. This iSBX connector will be covered by the iSBC 309 board.

d. Carefully remove 8086 processor device from host CPU board socket.

e. Install 8086 processor device into iSBC 308/309 board socket U36. Ensure that the notched end of the 8086 faces resistors R1 - R4. If the 8087 Numeric Data Processor device is used, install it in iSBC 308/309 board socket U37 (leftmost socket).

f. Remove the plastic protective case from the iSBC 308/309 board connector P1. Inspect all pins for damage. Straighten any bent pins.

g. Using two of the spacers and screws provided, install them to the solder side of the iSBC 308/309 board, as shown in Figure 2-3.

h. Refer to Figure 2-4. Carefully insert iSBC 308/309 connector P1 into host CPU socket (processor socket), as shown in Figure 2-4. Ensure that all pins are properly seated. Press down on the iSBC 308/309 board until it is firmly locked in place, and the two spacers are flush to the host CPU board surface.

i. Secure the spacers to the host CPU board by installing two screws from the solder side of the host CPU board (see Figure 2-3).

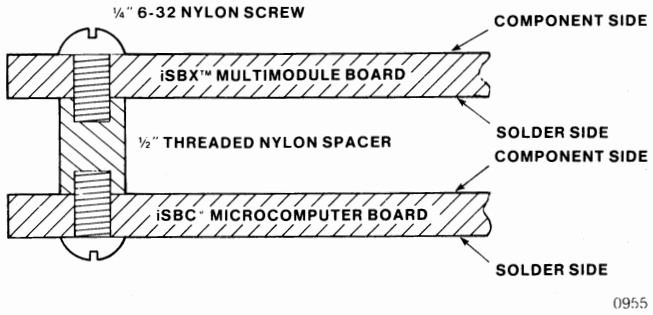


Figure 2-3. iSBC® 308/309 Mounting Technique

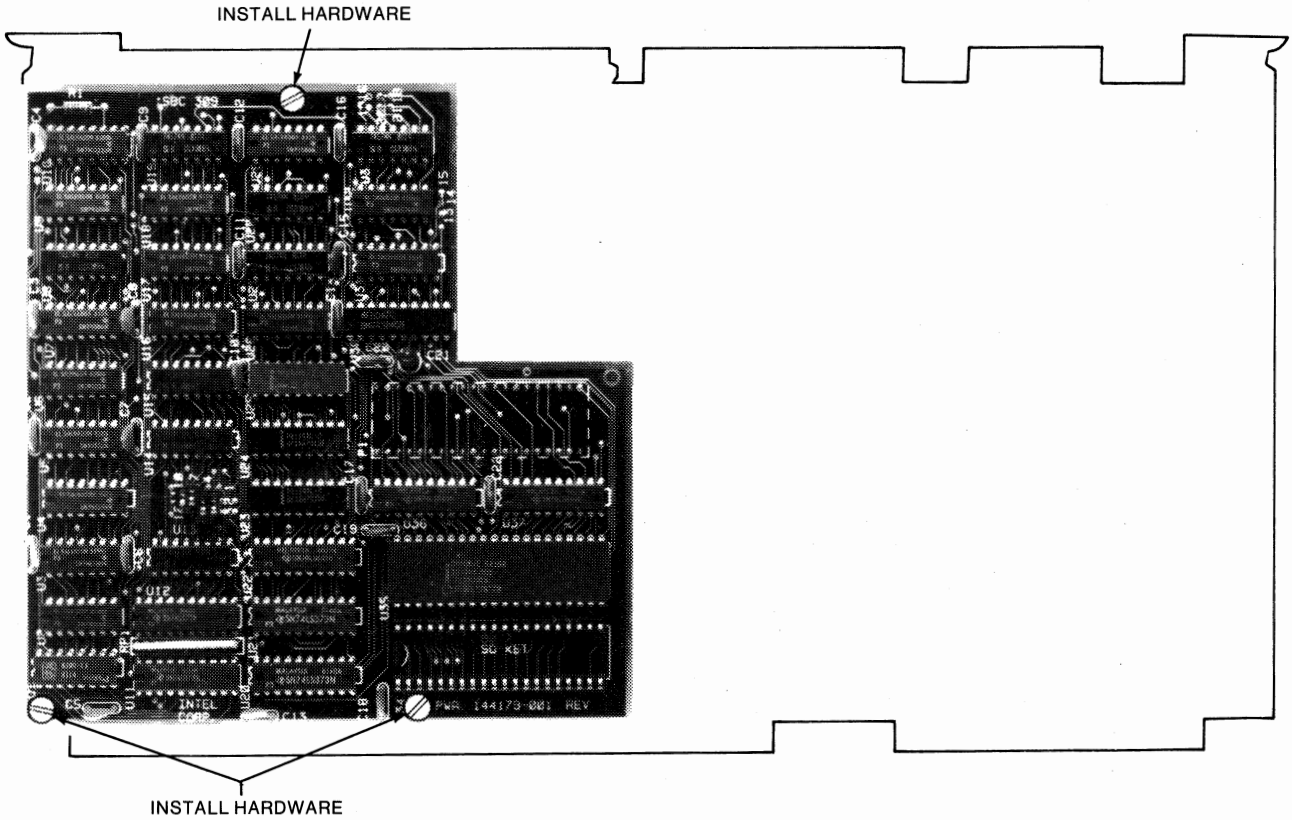


Figure 2-4. iSBC® 309 Board On iSBC® 86/30 Board

2.5 iSBC 308/309 JUMPER OPTIONS

2.5.1 USER MODE I/O OPTION

Direct user mode I/O is enabled or disabled according to jumper configuration. If jumper 14 - 15 is installed, no user I/O is allowed, except via the System Call Command. In this mode all I/O operations must be performed by a system mode process. If jumper 14 - 15 is removed and 13 - 14 installed, direct unrestricted I/O is allowed in the user mode.

2.5.2 NUMBER OF CONCURRENT PROCESSES OPTIONS

As shown in Section 1.2, there is a direct relationship between the number of processes mapped at one time, and the logical memory size for each process. For each configuration listed, the Process Register format is slightly different. The format shown is Section 3.3.2 is the standard configuration of eight processes. Table 2-1 shows the different jumper options and processes available. Each of the lower five bits of the Process Register correspond to either one of the upper logical address lines, L10 - L13 (used only when programming the memory map), or to one of the process selection bits. The bits that correspond to upper logical address line bits are used to select in which 64K block a particular page resides (Table 2-2).

Table 2-1. Process Selection Jumpers

Number of Process Maps	Connect 2 to	Connect 5 to	Connect 8 to	Connect 11 to
2	1	4	7	10
4	3	4	7	10
8*	3*	6*	7*	10*
16	3	6	9	10
32	3	6	9	12

Note: * = Factory default jumper configuration.

Table 2-2. Process Register Format

Number of Processes	Data Bus					
	D5	D4	D3	D2	D1	D0
2	EM	PR0	L13	L12	L11	L10
4	EM	PR1	PR0	L12	L11	L10
8	EM	PR2	PR1	PR0	L11	L10
16	EM	PR3	PR2	PR1	PR0	L10
32	EM	PR4	PR3	PR2	PR1	PR0

CHAPTER 3
PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter describes the command format used for programming the iSBC 308/309 boards. The chapter also describes how commands can be used to handle various memory management events. The following topics are discussed: how to initialize a device; how to service interrupts and handle traps; and the sequence for switching between a user process and a system process.

3.2 NOTATION AND DEFINITIONS

Hexadecimal notation is used to describe 8086 address and data bus bits with 0 being the least significant bit.

3.2.1 LOGICAL ADDRESS

The 20 bits of the logical memory address are designated as L0 through L13 (hexadecimal).

3.2.2 PHYSICAL ADDRESS

The 20 bits of the physical memory address are designated as P0 through P13 (hexadecimal).

3.2.3 PAGE CONCEPT

A page of memory is a contiguous 2K byte block of memory which can begin on any 2K byte boundary (integer multiple of 2K). A page represents the smallest segment of memory which can be independently memory mapped (assigned).

There are 32 logical address pages per 64K byte block. These pages are labeled 0 - 31 (decimal) with 0 being the lowest page value in the block. In the eight-process (Xenix operating system) configuration there are four 64K byte blocks per process, for a total of 128 pages per process. Thus, each logical page within a process is denoted by a page number (0-31) and a block number (0-3). Figure 3-1 illustrates this concept.

Every accessible logical page has a corresponding physical page. There are a total of 512 2K byte physical pages, denoted as 0 - 511 decimal.

3.2.4 PROCESS CONCEPT

A process is defined as any software function which has its own logical map, independent of other process maps. In the eight-process (Xenix) configuration, up to eight processes can reside in the system memory map at one time. The number of the process currently executing is held in the process register.

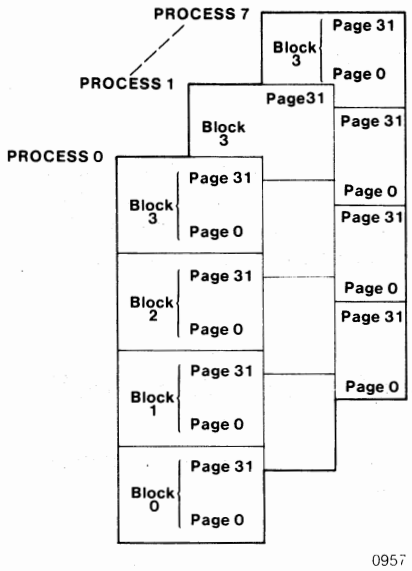


Figure 3-1. Logical Page Notation

3.2.5 TRAP CONCEPT

A trap on the iSBC 308/309 boards is a recognized non-maskable interrupt. Trap interrupts are initiated after a low-to-high level transition at the NMI input on the 8086 microprocessor. A trap interrupt occurs whenever the Trap Flag is set. The Trap Flag is set by a process executing a System Call command, or when an exception (invalid operation) occurs (see section 3.2.6).

3.2.6 EXCEPTIONS

An execption occurs whenever a process performs an invalid operation. When this happens, the current instruction is aborted, the Trap Flag is set, and control is passed to the operating system. The following exceptions can occur:

OPERATION:	CONDITIONS:
Input/Output	In the User Mode, all I/O is invalid, except the System Call command, Clear Status, and the Set/Clear System Mode command. (All I/O is valid in the System Mode).
Masking Interrupts	Disabling interrupts while in User Mode is invalid. (Valid in System Mode).
Memory Reference	Referencing a logical page in a manner which violates the page access code. (User and System mode).

3.2.7 SYSTEM REQUEST FLAG

The System Request flag is set whenever a System Call command is executed. The flag is used to indicate the occurrence of a valid request, rather than an execption. The flag is cleared by the Clear Status Command.

3.2.8 SYSTEM/USER MODE

The System Mode refers to any iSBC 308/309 state where the System Mode flag is set. The User Mode is any state where the flag is reset. The two modes differ in one major respect: interrupts can be disabled in the System Mode, but not in the User Mode. In addition, all I/O operations are invalid in the User Mode (see section 3.2.6).

3.2.9 iSBC 308/309 I/O SPACE

All iSBC 308/309 functions are performed using I/O commands. A 64K byte user I/O space and a 64K byte system I/O space exist for this purpose. Both the user and system I/O space are divided into 1K byte blocks which are assigned to various iSBC 308/309 functions. In the eight-process (Xenix) configuration all user mode I/O is invalid, except system calls. I/O functions with addresses that are outside the reserved space are available for general use. In the System Mode, all odd 1K byte blocks are dedicated to programming the memory map.

Every logical 2K byte page in the logical address space has a corresponding I/O port address. For example, port 0400 (hexadecimal) corresponds to logical addresses 0 - 07FF (page 0, block 0). Figure 3-2 lists the I/O port assignments for the User and System Modes.

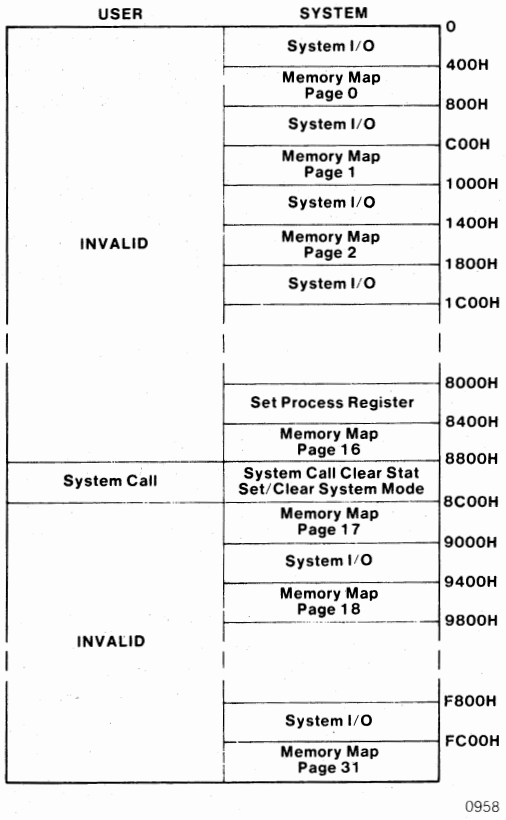


Figure 3-2. iSBC® 308/309 User & System I/O Space

The remaining 32K bytes of System Mode I/O space are available for general use, except for two 1K byte blocks which are used for setting the Process Register and the System Call command. Because I/O is limited to 64K bytes, only 32 pages of logical memory are directly mapped. Different 64K byte segments are selected by placing the upper address bits in the Process Register. (See section 3.4.2.)

3.3 COMMANDS

Commands issued to the iSBC 308/309 boards are in 16-bit word I/O read or write form. In some cases an I/O read command will return the current status. The following sections provide command format information.

3.3.1 MAP MEMORY COMMAND (SYSTEM MODE ONLY)

Input/Output Word Format:

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Address:	LF	LE	LD	LC	LB	1	X	X	X	X	X	X	X	X	X	0
Data:	PF	PE	PD	PC	PB	X	X	X	SR*	TR*	RD	WR	P13	P12	P11	P10

X = Irrelevant Bit; * = Input Only

PB - P13: These bits represent the part of the physical address which corresponds to the logical address LB - LF. The upper logical address bits are set by the Process Register command.

RD, WR: These two bits are used to set the access code for each logical page to allow read operations, write operations, both, or neither. An instruction fetch is considered a read cycle. The following table defines RD, WR bit programming:

RD	WR	DESCRIPTION
0	0	Invalid; causes an exception.
0	1	Write only; any read causes an exception.
1	0	Read only; any write causes an exception.
1	1	Read/Write; any read or write cycle allowed.

SR, TR: Input only. These two hardware flags indicate the status of the iSBC 308/309 board. The SR bit is the System Request Flag, which is set whenever a System Call command is performed. The TR bit, when set, indicates that a trap interrupt has occured. Notice that the status of the Enable Memory Management Flag and the System Mode Flag, are not accessible. Therefore the status of these two flags should be saved by software. The SR and TR flags are valid when any part of the memory map is read. The following table defines SR, TR bit programming.

SR	TR	DESCRIPTION
0	0	User Mode (or System mode after Clear Status Command).
0	1	Exception has occurred.
1	0	Maskable interrupt has occurred.
1	1	System Call command has occurred.

3.3.2 SET PROCESS REGISTER COMMANDS (SYSTEM MODE ONLY)

Output Word Format (eight-process configuration):

Word Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Address:	1	0	0	0	0	0	X	X	X	X	X	X	X	X	X	0
Data:	X	X	X	X	X	X	X	X	X	X	EM	PS2	PS1	PS0	L11	L10

X = Irrelevant Bit

L10, L11: These bits are used to select which 64K byte block is being programmed in the memory map. There are four blocks (0-3) for each process. These bits are used only when programming the memory map.

PS0, PS1,PS2: These bits designate which process is active (of the eight possible processes which can be mapped concurrently). They are used for selecting which section of the memory map to use for program execution and programming the memory map.

EM: Enable Memory Management. When the Enable Memory Management bit is true, the physical memory address is generated by the memory map. When the EM flag is false, the physical memory address comes directly from the 8086 microprocessor and the memory map is disabled. To use non-mapped operating systems such as Intel's iRMX 86 Operating System, EM should be 0.

EM = 0 Disable memory address mapping
EM = 1 Enable memory address mapping

3.3.3 SYSTEM CALL COMMAND (SYSTEM/USER MODE)

Output Word Format:

Word Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Address:	1	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X
Data:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Irrelevant Bit

The System Call command is made by a process to request service from the operating system. The command indirectly sets the Trap flag and the System Request flags discussed in section 3.3.1. Setting the Trap flag causes the CPU to trap and transfer control to the operating system.

NOTE

The NMI input on the 8086 CPU is dedicated to the iSBC 308/309 board. The host board cannot use the NMI function in this configuration.

3.3.4 CLEAR STATUS COMMAND (SYSTEM/USER MODE)

Input Word Format:

Word Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Address:	1	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X
Data:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Irrelevant Bit

The Clear Status command resets the Trap and System Request flags discussed in section 3.3.1. The command can be executed in either the System Mode or the User Mode. (However, this command has no effect in the User Mode since the flags are cleared in that mode.)

3.3.5 SET/CLEAR SYSTEM MODE COMMAND (SYSTEM/USER MODE)

Input/Output Word Format:

Word Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Address:	1	0	0	0	1	0	1	X	X	X	X	X	X	X	X	X
Data:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Irrelevant Bit

This command sets or resets the System Mode Flag according to the condition of the Trap flag. The command has no effect in the User Mode. Thus, a trap interrupt must occur before the System Mode flag can be set.

TRAP FLAG	DESCRIPTION
0	System Mode flag is reset
1	System Mode flag is set

CAUTION

If TR = 1 all other trap-causing events are essentially masked off. No other traps will occur in this mode.

3.4 SYSTEM SOFTWARE CONSIDERATIONS

The following sections describe system initialization, process switching, trap handling, and interrupts.

3.4.1 INITIALIZATION

After a hardware reset (INIT/), the iSBC 308/309 disables the memory map and sets the hardware flags as follows:

EM:	0
System Mode:	1
System Request:	1
Trap:	0
Process Number:	0

After reset, three tasks must be performed before the memory map can be enabled and control passed to the normal operating system mode. These tasks must be performed by the initialization software.

The first task is to map page 0 of block 0 into the same physical page for all processes. This page should be marked as read-only for all User Mode processes and as read/write for the System Mode process. The page should be marked as read-only for the User processes because it will contain the system interrupt vectors as well as any system functions which require changing the memory map. Thus, this page should not be altered by a user program. Figure 3-3 shows a typical mapping scheme.

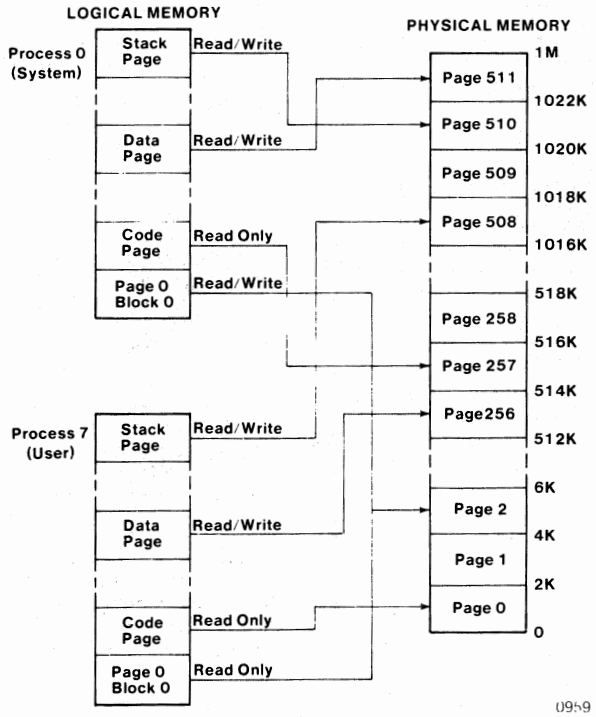
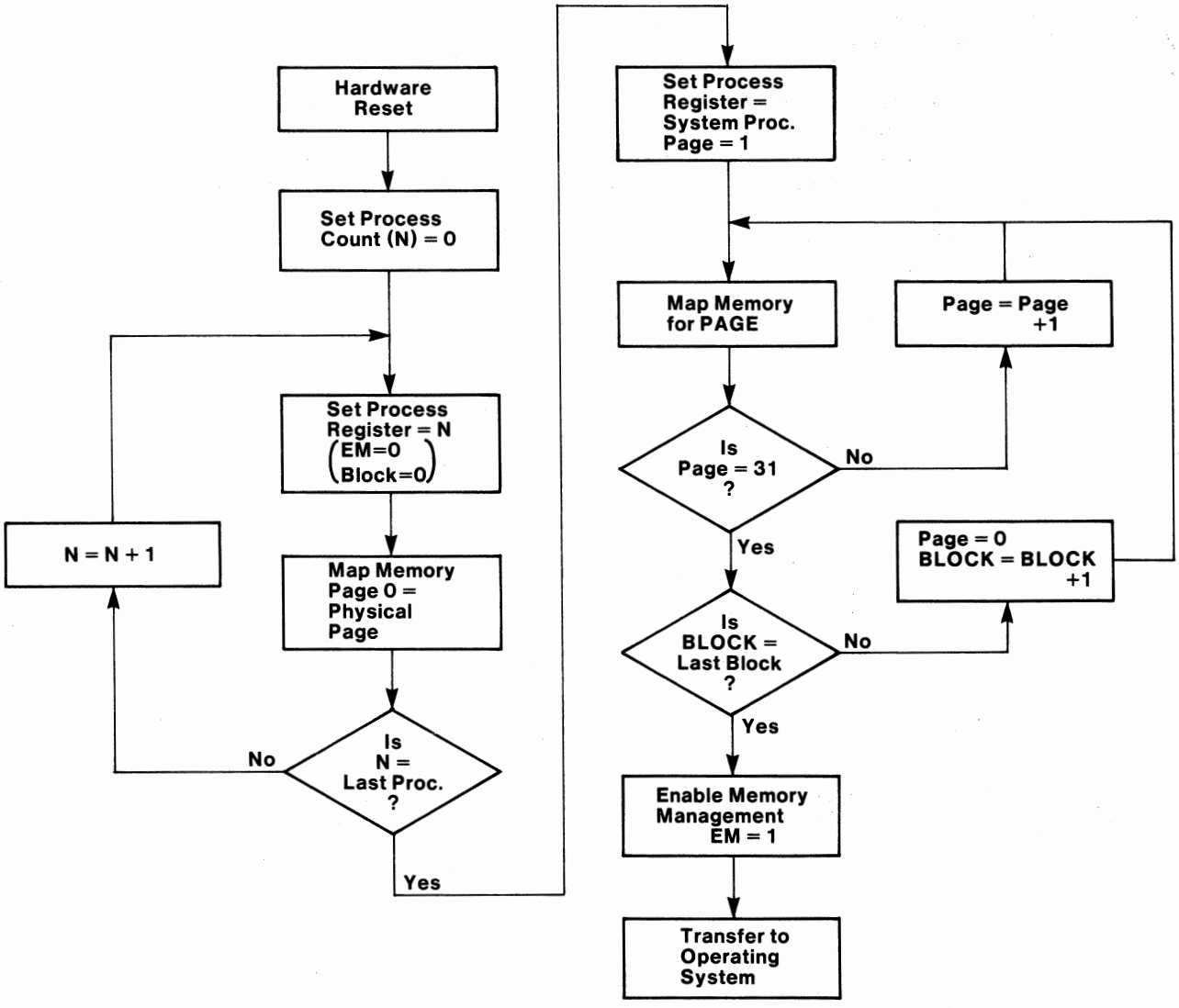


Figure 3-3. Example Memory Map

Secondly, if the system is RAM based, an operating system kernal will have to be loaded into memory. Finally, the rest of the system process memory map must be programmed. At that point the memory map can be enabled.

The key point when enabling the memory map is that the software should be executing in a page in memory whose logical addresss is identical to its physical address. This one-to-one mapping is necessary to avoid any discontinuity in the instruction stream when the memory map is enabled. This same point would also apply when disabling the memory map. Figure 3-4 illustrates a typical initialization process. In most cases, the operating system will perform many of the iSBC 308/309 initialization requirements.


Hardware Reset
Set Process Count (N) = 0
Set Process Register = N (EM=0 Block=0)
Map Memory Page 0 = Physical Page
Is N = Last Proc. ?
No
Yes
N = N + 1
Set Process Register = System Proc. Page = 1
Map Memory for PAGE
Page = Page +1
Is Page = 31 ?
No
Yes
Page = 0 BLOCK = BLOCK +1
Is BLOCK = Last Block ?
No
Yes
Enable Memory Management EM = 1
Transfer to Operating System

Note: Typically the operating system performs iSBC 308/309 board initialization.

0960

Figure 3-4. Typical Initialization

3.4.2 PROCESS SWITCHING

Whenever the process number in the Process Register is changed, a different section of the memory map is addressed. In order to change the Process Register without jumping from one software routine to another, the program that changes the register must be executing in a logical page which is mapped into the same physical page for both the current process and the new process. Figure 3-5 illustrates this mapping scheme.

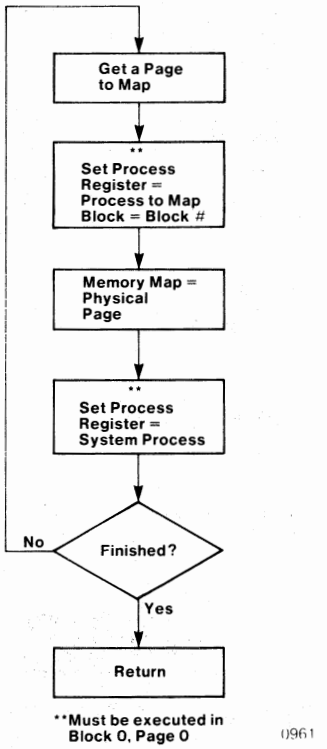


Figure 3-5. Typical Memory Mapping Routine

As discussed in Section 3.4.1, logical page 0 block 0 must be mapped into the same physical page for all processes. Therefore, locating all functions which actually change the process number in logical page 0 block 0 will solve this problem. Note that any data or stack information required when switching between two processes must also be located in a shared page.

There are three situations in which the Process Register needs to be changed. The first involves programming the memory map. The Process Register has to be loaded with the process number of the map being changed. This function must be located in block 0 page 0 or in some other shared page. Figure 3-5 is a simplified flow chart of a section of a typical memory map program.

The second situation where the Process Register needs to be changed is when switching program control from the system process to a user process. Figure 3-6 illustrates this procedure. Assume here that the register contents and flags were saved on the user stack before control was transferred to the operating system. Thus, if the user process stack pointer is restored, the program context can also be restored. This procedure allows a process to be restarted. Note that interrupts are enabled *after* entering the User Mode. Interrupts are enabled with IRET.

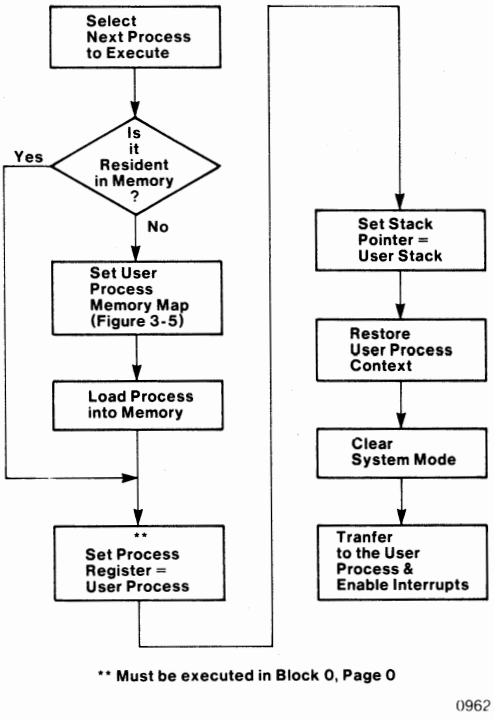

Select Next Process to Execute
Is it Resident in Memory ?
Yes
No
Set User Process Memory Map (Figure 3-5)
Load Process into Memory
**
Set Process Register = User Process
Set Stack Pointer = User Stack
Restore User Process Context
Clear System Mode
Tranfer to the User Process & Enable Interrupts
** Must be executed in Block 0, Page 0
0962

Figure 3-6. Typical Procedure For Activating A User Process

CAUTION

When switching to the User Mode, interrupts must be disabled (off). This is necessary to prevent an excessive number of interrupt requests from being stored on the User stack.

The third situation where the Process Register needs to be changed is when control is switched from a User Mode process to the operating system. As illustrated in Figure 3-7, this occurs as a result of an exception, a System Call command, or an interrupt.

3.4.3 TRAP HANDLERS

An 8086 trap interrupt (NMI) occurs whenever the Trap Flag is set. The Trap Flag is set by an exception or a System Call command. The following sections describe the events which cause the Trap Flag to be set.

3.4.3.1 Exceptions

An exception occurs in a User or System Mode process whenever a memory reference is made to a logical page which violates the access code. The access code is set in the memory map for each page as described in section 3.3.1. An exception can

also occur in the User Mode if interrupts are disabled or an I/O operation is attempted. When an exception occurs, the iSBC 308/309 sets the Trap Flag and aborts the bus cycle by disabling the 8086 status lines.

After the 8086 recognizes the trap, it will push its flags and instruction pointer onto the User stack, disable interrupts, and then transfer control to trap handling software. The starting address of this software is located in memory at locations 8 - 11 (decimal). As shown in Figure 3-7, the trap handler saves the rest of the registers on the user process stack. The software then sets the system process, and saves the stack pointer (which now points to the user process register location). By reading the iSBC 308/309 status flags, as described in section 3.3.1, the system program can determine if the trap was generated by a valid System Call command. After inputting the status, the program should clear the status flags and then service the trap.

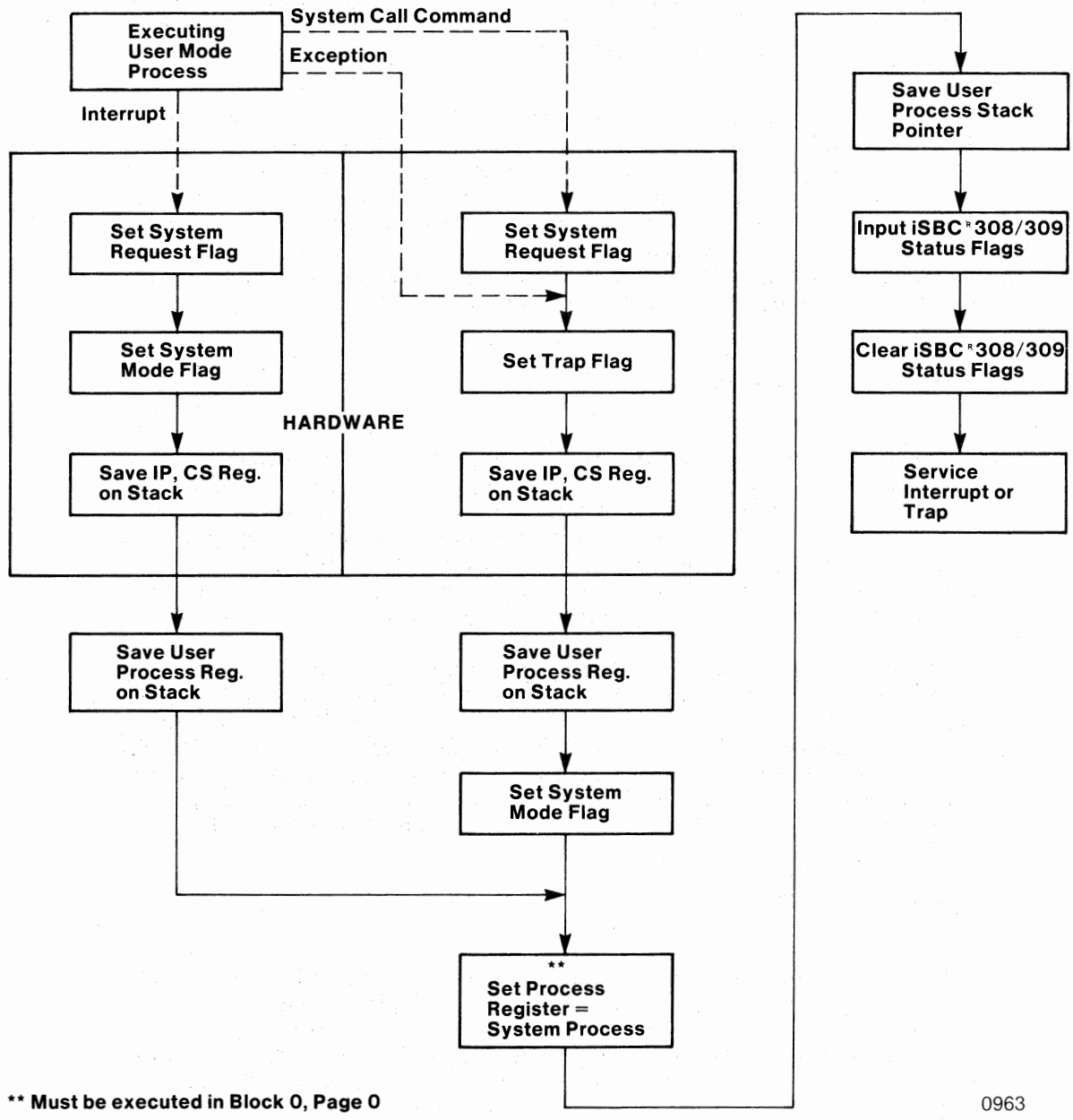

Executing User Mode Process
System Call Command
Exception
Interrupt
Set System Request Flag
Set System Mode Flag
Save IP, CS Reg. on Stack
HARDWARE
Set System Request Flag
Set Trap Flag
Save IP, CS Reg. on Stack
Save User Process Reg. on Stack
Save User Process Reg. on Stack
Set System Mode Flag
**
Set Process Register = System Process
Save User Process Stack Pointer
Input iSBC®308/309 Status Flags
Clear iSBC®308/309 Status Flags
Service Interrupt or Trap
** Must be executed in Block 0, Page 0
0963

Figure 3-7. Typical User Mode To System Mode Process

3.4.3.2 8086 Architecture Considerations

The 8086 microprocessor instruction queue requires special handling when servicing iSBC 308/309 trap interrupts. The 8086 uses a six byte instruction queue to prefetch instructions and operands. Where possible, for maximum efficiency, the 8086 will begin executing the next instruction while the the previous instruction is finishing. For example, if an instruction requires a write operation to a certain memory address, the 8086 will begin executing the next instruction while the write cycle is being performed.

If the next instruction requires no memory or I/O reference, then it may actually finish before the memory write cycle. Furthermore, if the memory write instruction was followed by several register-to-register transfer instructons, the 8086 may actually execute all of the register transfer instructons before the memory write cycle is complete (because of the queue structure).

The 8086 is five bytes ahead of the memory write instruction, causing a minor detrimental effect on the trap handler: the program counter might not point to the instruction which caused the trap. For instance, in the previous example, if the memory write cycle caused an exception, one or two of the register transfer instructions might execute before the trap is recognized. If a jump instruction were to follow the instruction causing the trap, then the instruction pointer would not accurately point to the offending instruction. Thus, it is sometimes impossible to know exactly where a process exception occurred.

3.4.3.3 System Calls

Whenever a process requires service from the operating system, such as a disk I/O operation, the process can voluntarily "trap" itself to the operating system to ask for service, by executing a System Call command. When the command is executed, the iSBC 308/309 sets the System Request Flag and the Trap Flag. Once the trap occurs, the trap handler reads the status flags to determine whether a System Call command or an exception had occurred. The request is serviced by the operating system, and then the process restarts as described in section 3.4.2.

Note that the 8086 instruction queue effects system calls and exceptions. One memory reference instruction and a maximum of two non-memory reference instructions can be executed after the System Call command. Thus, the software should provide one or two instructions following the call which can be executed before or after the System Call is serviced. Two NOP instructions could be used for this purpose in an assembly language program, or an assignment statement in a high level program such as an instruction that sets a variable equal to itself.

3.4.3.4 Interrupts

The final way to exit a process (enter the operating system) is for a maskable interrupt to occur. When the 8086 recognizes this interrupt, it generates two interrupt acknowledge cycles, during which the processor reads the interrupt vector. At the end of the first acknowledge cycle, the iSBC 308/309 board sets the System Request Flag and the System Mode Flag. After these two cycles the 8086 saves the state of its flags and instruction pointer, just as it does for a trap.

The starting address for an interrupt is located in an array of pointers located in the lower 1K of logical memory. This lower page of memory should be write-protected

so that the user process cannot alter it. Therefore, the system process must provide the interrupt vectors that the user process will use.

Generally, real-time interrupts are used in a multitasking system to limit the amount of time any process can run. For instance, every 50 msec. an interrupt could be generated to pass control from one user process to the next via the operating system. If a user process could disable interrupts then the 50 msec. time limit could be circumvented since a user process might not ever give up control.

To avoid this, the iSBC 308/309 board does not allow a user process to disable interrupts (they can be previously disabled in the System Mode). If a user process disables interrupts an exception will occur immediately. Another point is that the System Mode Flag is already set by the hardware when an interrupt occurs. Hence, the software should not execute a Set/Clear System Mode commmand after an interrupt. This procedure is outlined in Figure 3-7.

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This chapter provides a functional description of iSBC 308/309 board operation, AC & DC characteristics of the board, and the pre-programmed PROM map.

4.2 GENERAL DESCRIPTION

The iSBC 308/309 board provides memory management and memory protection for the iSBC 86/12A board, iSBC 86/14 board, and the iSBC 86/30 board. It does this by first examining the address generated by the 8086 CPU at the beginning of every cycle. If the address is invalid then the exception logic will abort the operation and cause a trap to occur.

Because of the additional time required to examine and translate the 8086 CPU cycle, the system requires a delay until later in the cycle. The function of the iSBC 308/309 board is to add wait states (idle states) to the beginning of each bus cycle. One wait state is inserted at 5MHz and two wait states are inserted at 8MHz. The wait states are inserted by delaying the time in which the status lines are allowed to become active with the host board logic. This is shown in Figure 4-1. The inserted wait states (shown as TW in Figure 4-1) allow enough time for address translation and for the generation of a valid address at the proper time in the bus cycle (relative to the host board).

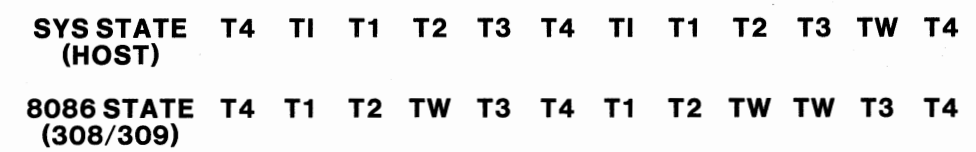


Figure 4-1. Host - iSBC® 308/309 Interface Timing

4.3 FUNCTIONAL DESCRIPTION

This section provides descriptions of the following functional areas of the board: system interface, timing logic, I/O decoding, mode control, exception logic, process register and memory map, and interface control. Refer to the schematic diagrams in Chapter 5 when studying this material.

In the descriptions below, the following signal notation convention is used: signals preceded by a "+" are active (true) in the high state (+5vdc); and signals preceded by a "-" are active (true) in the low state (0vdc). The source or destination of a particular signal on the schematic diagram is specified by a code which first states the schematic page number and then the grid zone on that page.

4.3.1 SYSTEM INTERFACE

The iSBC 308/309 board AC and DC characteristics are listed in Tables 4-1 and 4-2. In Table 4-1, only those timing parameters which are different from the published Intel 8086 specifications are listed.

Once the iSBC 308/309 board is installed on the host board, the 8086 CPU personality changes slightly. The following list outlines the changes:

a. The electrical interface is different for most 8086 pins. See Table 4-2.

b. Several timing parameters are different; see Table 4-1.

c. The non-maskable interrupt (NMI) is dedicated to the iSBC 308/309 board.

d. The 8086 must be in maximum mode. The minimum mode is not supported.

e. The RQ/GT function is not supported. This means that the local 8086 bus cannot be shared with another master. However the 8087 device is fully supported by the iSBC 308/309 board.

f. The 8086 RD line is not supported and is instead used to connect the 8087 INT signal to the 8086 system.

g. Pins 30 (RQ/GT0) and 31 (RQ/GT1) should be connected to +5vdc. Pin 33 (MN/MAX) should be connected to ground.

h. The upper status bits (S4 - S6) are not generated.

4.3.2 TIMING LOGIC

The timing logic decodes the 8086 status lines and generates the signals which denote the four processor states T1 through T4 that occur during a bus cycle. These timing signals are generated by shifting a single bit in a shift register every

Table 4-1. iSBC® 308/309 AC Characteristics

Symbol	Parameter	5MHz				8MHz			
		8086		308/309		8086-2		308/309	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
T_{DVCL}	Data In Setup Time	30		45		20		35	
T_{CHRYX}	Ready Hold Time	30		0		20		0	
T_{RYLCL}	Ready Inactive to CLK	-8		0		-8		0	
T_{RYHSH}	Ready Active to Status Passive		110		145		65		100
T_{CHSV}	Status Active Delay	10	110	10	130	10	60	10	65
T_{CLSH}	Status Inactive Delay	10	130	10	150	10	70	10	90
T_{CLAV}	Address Valid Delay	10	110	10	55	10	60		0
T_{CLAX}	Address Hold Time	10		60	55	10		40	
T_{CLAZ}	Address Float Delay		80		95		50		80
T_{CLDV}	Data Valid Delay	10	110	10	110	10	60	10	90

clock cycle while the status is active. The shift register is implemented with a 74S175 (U3) found at 2B2. Signal -T4 is active during the last clock cycle of a bus cycle and during any idle cycles. Signal -T4 is generated by flip-flop (FF) U14, which is cleared on the falling edge of the processor clock after status becomes inactive.

When the status becomes active, as indicated by +ACTIVE, FFU3 starts being clocked. This generates +T1 which signals the start of an active bus cycle. Signal +T1 becoming active presets FFU14 which drives Signal -T4 inactive. The next clock cycle after +T1 causes +T2 to become active and +T1 becomes inactive. Likewise, at the next clock cycle, +T3 becomes active and +T2 becomes inactive. Finally, +T3 becomes active and all three signals remain inactive until a new bus cycle is initiated. At the beginning of a new bus cycle, FFU7 at 2B2 gets set for half a clock cycle. This produces +ALE which is used to latch the 8086 address.

Table 4-2. iSBC® 308/309 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	MIN	MAX	Units
CLK	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.5V		-0.4	mA
	I_{IH}	Input Current at High V	V_{IN}=2.7V		50	uA
	C_L	Capacitive Load			15	pF
READY	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.5V		-2.0	mA
	I_{IH}	Input Current at High V	V_{IN}=2.7V		50	uA
	C_L	Capacitive Load			15	pF
RESET	V_{IL}	Input Low Voltage			0.4	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.5V		-2.4	mA
	I_{IH}	Input Current at High V	V_{IN}=2.7V		110	uA
	C_L	Capacitive Load			20	pF
S0,S1,S2	V_{OL}	Output Low Voltage	I_{OL}=20mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH}=-1mA	2.7		V
	C_L	Capacitive Load			15	pF
AD0-AD15	V_{OL}	Output Low Voltage	I_{OL}=2.1mA		0.4	V
AD16-AD19	V_{OH}	Output High Voltage	I_{OH}=-1mA	2.4		V
	V_{IL}	Input Low Voltage			-0.6	V
	V_{IH}	Input High Voltage		2.0	0.45	V
	I_{IL}	Input Current at Low V	V_{IN}=0.40V		150	mA
	I_{IH}	Output Leakage High	V_O=5.25V		20	uA
	C_L	Capacitive Load			20	pF
LOCK,BHE,	V_{OL}	Output Low Voltage	I_{OL}=2.0mA		0.45	V
QS0, QS1	V_{OH}	Output High Voltage	I_{OH}=-.4mA	2.4		V
8087 INT	I_{LH}	Output Leakage High	V_O=5.25V		10	mA
	I_{LL}	Output Leakage High	V_O=0.45V		-10	uA
	C_L	Capacitive Load			10	pF
INTR	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN}=0.45V		-10	uA
	I_{IH}	Input Current at High V	V_{IN}=5.25V		10	uA
	C_L	Capacitive Load			10	pF

Signal -STEN determines the time in which the system status lines are allowed to become active. It is produced by FFU36 at 3B2 and becomes active at the beginning of T2 for 5MHz and the middle of T2 for 8MHz. It remains active until FFU36 is preset at the beginning of clock cycle T4. The final timing logic function is to delay the ready signal to ensure that the minimum number of wait states are inserted (one for 5MHz and two for 8MHz). This wait state(s) is needed to allow for delaying the start of the bus cycle. FFU9-5 at 2B2 is used to qualify the ready acknowledgement from the system by generating -RDY EN.

Signal -RDY EN becomes active in the middle of state T3 for 5MHz and one cycle later for 8MHz. When -RDY EN and +READY from the system are active then FFU9-9 is preset. This FF generates the 8086 ready signal. During iSBC 308/309 board function IO cycles and during aborted bus cycles, the iSBC 308/309 board must generate its own acknowledge. These two possible conditions are OR'ed together by the 74S32 (U13) located at 2C4 and are used to set FFU9-9 as soon as -RDY EN becomes active. The ready FF is set, in this case, by the falling edge of the CPU clock.

4.3.3 I/O DECODER

As shown in Figure 3-2, the iSBC 308/309 board creates two different I/O spaces—one for the system mode and one for the user mode. The heart of the decoder is a 256 X 4 bit bipolar PROM (U15) at 3A1 which assigns 1k byte blocks of I/O addresses either to one of three basic iSBC 308/309 board functions, or to the 8086 system. In addition to addresses ABA through ABF, the PROM address consists of the signal +S/U, which is high when in the system mode, and also a signal which is low during I/O cycles. (See Table 4-3 for PROM Map).

Table 4-3. Decode Prom Map

Upper Address	Lower Address															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
1	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
2	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
3	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
4	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
5	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
6	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
7	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
8	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
9	7	D	E	E	E	E	E	E	E	E	E	E	E	E	E	E
A	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
C	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
D	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
F	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E

Output	Function
E	Non-iSBC 308/309
D	Mode Control
7	Process Register
B	Memory Map

1K X 4 bit Bipolar PROM

The iSBC 308/309 board timing ensures that the PROM address does not change while it is enabled to avoid glitches on the outputs. The four signals that the PROM produces are -PROC CS, -MAP CS, -TRAP CS, and +LOC IO. During non-I/O cycles, all four signals are inactive. Signal +LOC I/O is a signal which is active during any iSBC 308/309 board function I/O cycle. During such cycles, +LOC IO disables the status lines and generates a local ready acknowledge in the same manner as an aborted cycle. Signal +LOC IO is OR°ed with the abort cycle signal with U13 at 2C4. The PROM is enabled by the signal -STEN. When -STEN is inactive, the PROM is disabled and all the outputs are high. Thus, when the status enable signal, -STEN, is inactive, +LOC IO is held active. This, in turn, inhibits the status lines from becoming active. When the PROM is enabled, +LOC IO will become inactive for non-iSBC 308/309 board I/O cycles, allowing the system status to become active.

For iSBC 308/309 board cycles, +LOC IO remains active and one of the other three outputs becomes active. Signal -STEN becomes inactive during cycle T4, and thus disables the PROM. The other three outputs are used as follows. The rising edge of -PROC CS is used to sample the data bus when changing the Process Register. The signal -MAP CS is active whenever the memory map is programmed. Every odd 1K block (ABA=1) is dedicated for memory map addressing. The final signal, -TRAP CS, indicates one of two different mode-related functions and must be decoded further in conjunction address line AB9. Nand gates U5 at 3B1 provide this decoding. With AB9 low, and -TRAP CS active, the TRAP and SYS RQT FFs are clocked. With AB9 high, the system mode FF is clocked.

4.3.4 MODE CONTROL

The mode control logic creates the system and user modes and generates the non-maskable interrupt (NMI) whenever a trap occurs. The logic consists mainly of the three FFs, U7-5, U6-5 and U6-9 located at 3C2 in the schematic. U7-5 generates the +TRAP signal, which becomes active whenever a NMI needs to be generated. U6-5 produces the +SYS RQT, which indicates that a System Call Command has occurred. Signal +S/U is generated by U6-9 and is active when the iSBC 308/309 board is in the system mode. The TRAP FF can be set in one of two ways. It can be preset during clock cycle T3 if an exception has occurred, or it can be clocked during a System Call by +TRAP CS (with AB9=0). The rising edge of +TRAP causes the CPU to recognize a NMI. (Since NMI is edge sensitive, +TRAP FF cannot cause another interrupt until it is cleared and set again).

The SYS RQT FF can either be clocked by +TRAP CS or it can be preset by an interrupt acknowledge cycle during clock cycle +T4. An interrupt acknowledge cycle occurs after the CPU recognizes a maskable interrupt. During this cycle, the status lines are decoded by half of multiplexer U10 at 2C3. The multiplexer produces -INTA CYC which is active during interrupt acknowledge cycles. In addition to the SYS RQT FF, -INTA CYC also presets the system mode FF. Thus, acknowledging an interrupt automatically sets the system mode with the SYS RQT flag set. The system mode FF, U6-9, can also be clocked by -TRAP CS (AB9=1).

On the rising edge of -TRAP CS (state T4), the FF samples the state of the +TRAP flag. Therefore, with the exception of an interrupt acknolwedge cycle, the system mode FF cannot be set unless the TRAP FF has been previously set. When the TRAP and SYS RQT FFs are clocked by -TRAP CS, they both sample the +WRITE signal. Signal +WRITE is active for write cycles so that the FFs are both set for an output cycle (System Call Command) and are both cleared for an input cycle (Clear Status Command). Note that multiplexer (U10) also generates

the -INTA CYC signal whenever a hardware reset occurs. Thus, the system request and system mode FFs are both set after a reset just as they are during an interrupt acknowledge cycle. In addition to this, the TRAP FF is cleared by a hardware rest.

4.3.5 EXCEPTION LOGIC

The purpose of the exception logic is to examine the type of bus cycle being attempted and to abort the bus cycle and generate a trap if a violation occurs. The lower half of the 74S253 multiplexer (U10 at 2C4) decodes the status lines S1, and S2 such that the four inputs into the multiplexer correspond to the memory read, memory write, I/O read, and I/O write operations. The output of the multiplexer is qualified with whether memory management is enabled or not. If memory management is disabled, then the exception logic will not cause an abort regardless of the output of U10. If the qualified abort signal is active, then the system status lines, -S0, -S1, and -S2 will be held inactive by gates U13 at 2D3. The status (held inactive) forces the iSBC 308/309 board ready logic to generate its own acknowledge rather than one from the system.

Also, +ABORT is active causing a trap to occur by setting the trap FF. For memory cycles, the two access code lines from the memory map, -BAD ADDR and -WR PROT are used. For memory read operations, a trap will occur if -BAD ADDR is active. For memory write operations, a trap will occur if -WR PROT is active.

For I/O operations, the multiplexer will generate an abort signal if and only if the user mode is set (+S/U inactive). While in the user mode, one I/O operation, the System Call Command, must still be valid. This one command is always allowed by qualifying the +ABORT signal with +TRAP CS. This logic, located at 3C1 prevents the TRAP FF From being preset when +TRAP CS is active. As stated earlier, the output of the multiplexer is qualified with an exception logic enable signal. If WW posts 14-15 are connected, as shown at 2A4, then the disable signal is -DIS FLAG. This signal is set directly in the Process Register.

If instead, jumper posts 13-14 are connected, then -DIS MM is used to disable the exception logic. Signal -DIS MM is the result of OR'ing together of -DIS FLAG and -IO. Signal -IO is active for I/O operations and interrupt acknowledge cycles. Thus, -DIS MM disables the exception logic during any I/O cycle. This allows I/O operations while in the user mode.

4.3.6 PROCESS REGISTER AND MEMORY MAP

The memory map logic takes the logical 8086 address, combined with the process number, and produces a physical address. The memory map itself is a 1K by 11 bit memory which consists of two 2114 RAMs (U24 and U28) and a 2149 RAM (U32). The 2149 is a faster RAM which is used to store the access code. The access code must be valid earlier in a cycle than the address itself to allow time for the exception logic to determine if the cycle must be aborted. The memory map logic is at 2C3 in the schematic and its address consists of the 8086 address (ABB through ABF) latched into the two 74S373s (U18, U20 at 2B1),, and the output of the Process Register logic (P0 through P4). P0 through P3 are multiplexed by 74S258 (U33) at 3B4. The multiplexer selects one of two different sources for P0 through P3. One source, consisting of the Process Register bits PS0 through PS3, is used when the memory map is being programmed (-MAP CS is active). The other source for the address comes, in part, from the upper 8086 logical address

lines AB10 through AB13 and, in part, from PS0 through PS3. This source is used whenever the map is not being programmed. The exact mixture of signals is determined by the number of processes selected by posts 1 through 12 located at 3B4.

For example, if sixteen processes are allowed to be mapped concurrently, then the upper address consists of AB10, P4, and PS1 through PS3. The purpose of the multiplexer is to allow PS0 through PS3 to be used to address the memory map concurrently. This switching of addresses is needed because I/O commands are used to program the memory map and I/O instructions can only address 64K of memory. Thus, the upper address lines, AB10 through AB13 cannot be set directly when mapping. Instead, the upper address lines that are used, if any, must be replaced with the corresponding Process Register bit when the map is set.

4.3.7 INTERFACE CONTROL

The interface control logic generates the system address/data bus. Because the iSBC 308/309 board demultiplexes the address/data bus from the 8086, the interface logic must multiplex the physical address and the data back again for the system interface. The upper nine address lines, ADB through AD13, are produced by the memory map (4B1) when it is enabled, or by buffers (U16, U29 at 4C1) whenever -DIRECT ADDR is active. This signal is active when -DIS MM is active (and the memory map is not being programmed). The lower address bus, AD0 through ADA, is driven by two 74S373s (U25, U26 at 4C2). The 74S373s latch the 8086 address and generate the system bus address regardless of whether the memory map is enabled, since the lower address lines are not affected by mapping.

The bus switches from address to data when +DATA EN becomes active. Signal +DATA EN is produced by FF U14-5 at 4A2 and it becomes active when the FF is set by -DEN. Signal -DEN is active during state T3 for 5 MHz and one clock cycle later for 8 MHz. The 74S153 (U31) at 4A3 controls the timing of the switch between address and data depending on the type of bus cycle. The four inputs to the multiplexer correspond to — programming the memory map while mapping is disabled, programming the map while mapping is enabled, normal bus cycle with mapping disabled, and a normal bus cycle with memory mapping enabled.

The upper multiplexer at U31 controls the enable for the two 2114s in the memory map. During programming cycles, the map is enabled for the entire cycle. For normal bus cycles, the map is enabled only until +DATA EN becomes active. Note that the part of the memory map that contains the access code data (U32) stays enabled for the entire bus cycle. It is only disabled during normal cycles when mapping is disabled. The lower half of the multiplexer controls the data transceiver. The data transceivers are only enabled after the address drivers are disabled to avoid any bus contention when switching back to address from data. For read cycles, the data bus is disabled at the beginning of T4 when FF U14 is clocked by +T4. For write cycles, FF U14 is cleared on the rising edge of the CPU clock during T4 - one half clock cycle later than for read operations. For normal bus operations, transcievers U21 and U22 at 4C3 are used to transfer data. For memory map programming cycles, transceivers U21 and U30 are used. For memory map read operations, U30 is also used to read the state of status lines +TRAP and +SYS RQT. These lines are driven only during read cycles by U16 at 4C4.

CHAPTER 5
SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides repair assistance information, a list of replacement parts, and a set of logic diagrams for the iSBC 308/309 boards.

5.2 SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other products, the serial number is usually stamped on a label.

d. Shipping & billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

Western Region	(602) 869 - 4951
Midwestern Region	(602) 869 - 4392
Eastern Region	(602) 869 - 4045
International	(602) 869 - 4391

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5.3 REPLACEMENT PARTS

Table 5-1 provides a list of iSBC 308 board parts; Table 5-2 provides a list of iSBC 309 board parts. The iSBC 308 board is shown in Figure 5-1; the iSBC 309 board is shown in Figure 5-2. The information in these tables and figures is subject to change without notice.

5.4 SCHEMATIC DIAGRAMS

A schematic diagram of the iSBC 308 board is provided in Figure 5-3, sheets 1 through 4; a schematic diagram of the iSBC 309 board is shown in Figure 5-4, sheets 1 through 4. These diagrams are subject to change without notice.

Table 5-1. iSBC® 308 Board Parts List

REF DESIGNATION	DESCRIPTION	QUANTITY
C1-7/9-11/13-19	Capacitor, .01uf Cer. Disk.	17
C8/12	Capacitor, 22uf Tant.	2
P1	Header Plug , 40-pin Gold Pin	1
P1	Socket, 40-pin Mach. Cont.	1
R1-4	Resistor, 1K ohm, 5%, .25W	4
R5	Resistor, 3.3K ohm, 5%, .25W	1
U1	IC, 74LS74	1
U2/13/19	IC, 74S32	3
U3	IC, 74S175	1
U4	IC, 74S02	1
U5/12	IC, 74LS00	2
U6/7/9/14/36	IC, 74S74	5
U8/17/27	IC, 74S00	3
U10/31	IC, 74S153	2
U15	IC, 6300 PROM	1
U16/29	IC, 74367A	2
U18/20	IC, 74S373	2
U21/22/30	IC, 74LS645	3
U23/11	IC, 74S04	2
U24/28	IC, 2114 RAM 120ns	2
U25/26	IC, 74LS373	2
U32	IC, 2149 RAM 55ns	1
U33	IC, 74S258	1
U34	IC, 74S174	1
U35	IC, 74S240	1
XU36/37	Socket, 40-pin Mach. Cont.	2

Table 5-1. iSBC® 309 Board Parts List

REF DESIGNATION	DESCRIPTION	QUANTITY
C1-20/22	Capacitor, .01uf Mono.	21
C21	Capacitor, 22uf Tant.	1
P1	Header Plug , 40-pin Gold Pin	1
P1	Socket, 40-pin Mach. Cont.	1
R1	Resistor, 3.3K ohm, 5%, .25W	1
RP1	Resistor Pack, 1K ohm, 5%, .25W	1
U1	MM86-2 PROM	1
U2	IC, 74S04	2
U3/26	IC, 74LS00	2
U4	IC, 74S258	1
U5	IC, 74LS32	1
U6	IC, 74S02	1
U7/9/29	IC, 74S00	3
U8/19/27/28/33	IC, 74S74	5
U10/16	IC, 74S153	2
U11/12	IC, 74S373	1
U13	IC, 74S174	1
U14/15	IC, 74367A	2
U17/18	IC, 74S32	2
U18/20	IC, 74S373	2
U20/21	IC, 74LS373	2
U22/36/37	IC, 74LS645	3
U23/24	IC, 2114 RAM 120ns	2
U25	IC, 2149 RAM 55ns	1
U30	IC, 74S240	1
U31	IC, 74S175	1
U32	IC, 74LS74	1
XU34/35	Socket, 40-pin Mach. Cont.	2

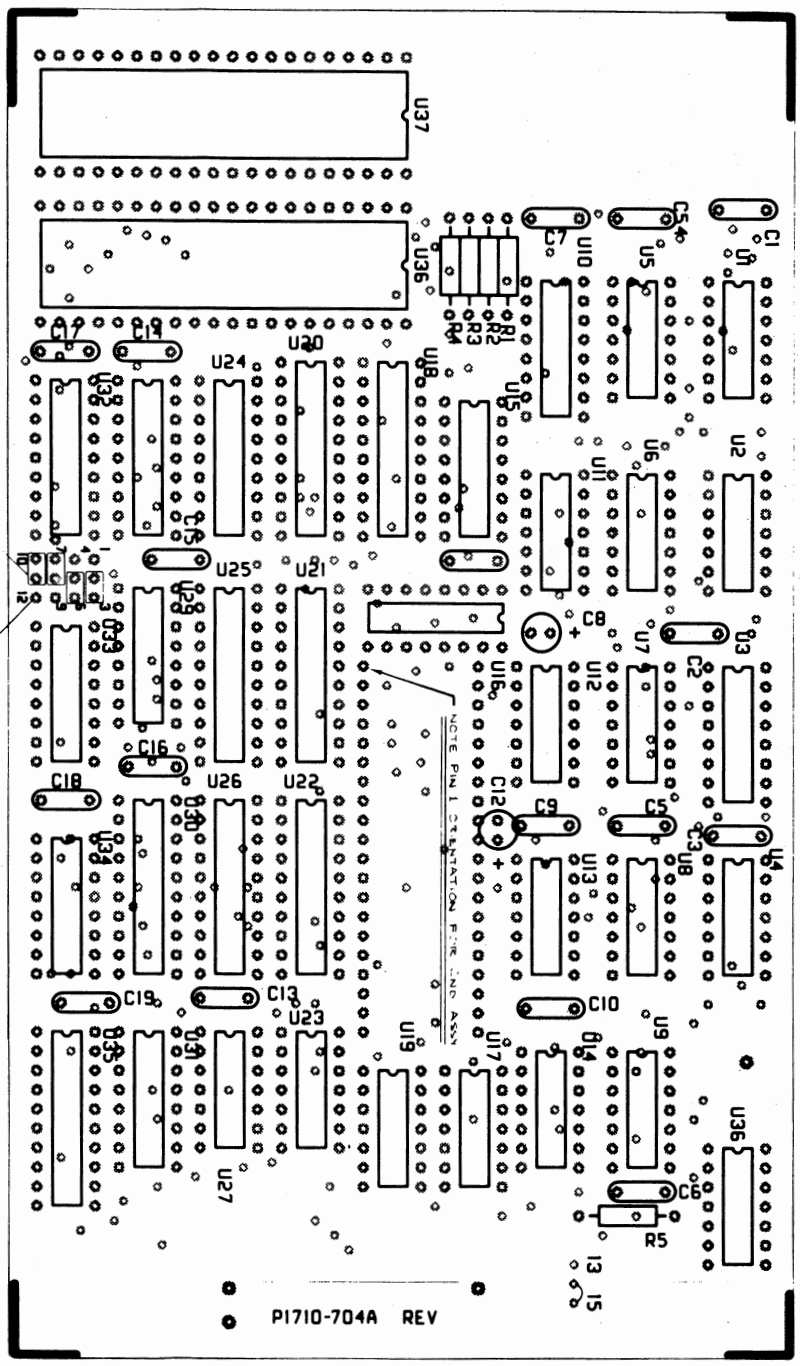


Figure 5-1. iSBC® 308 Board

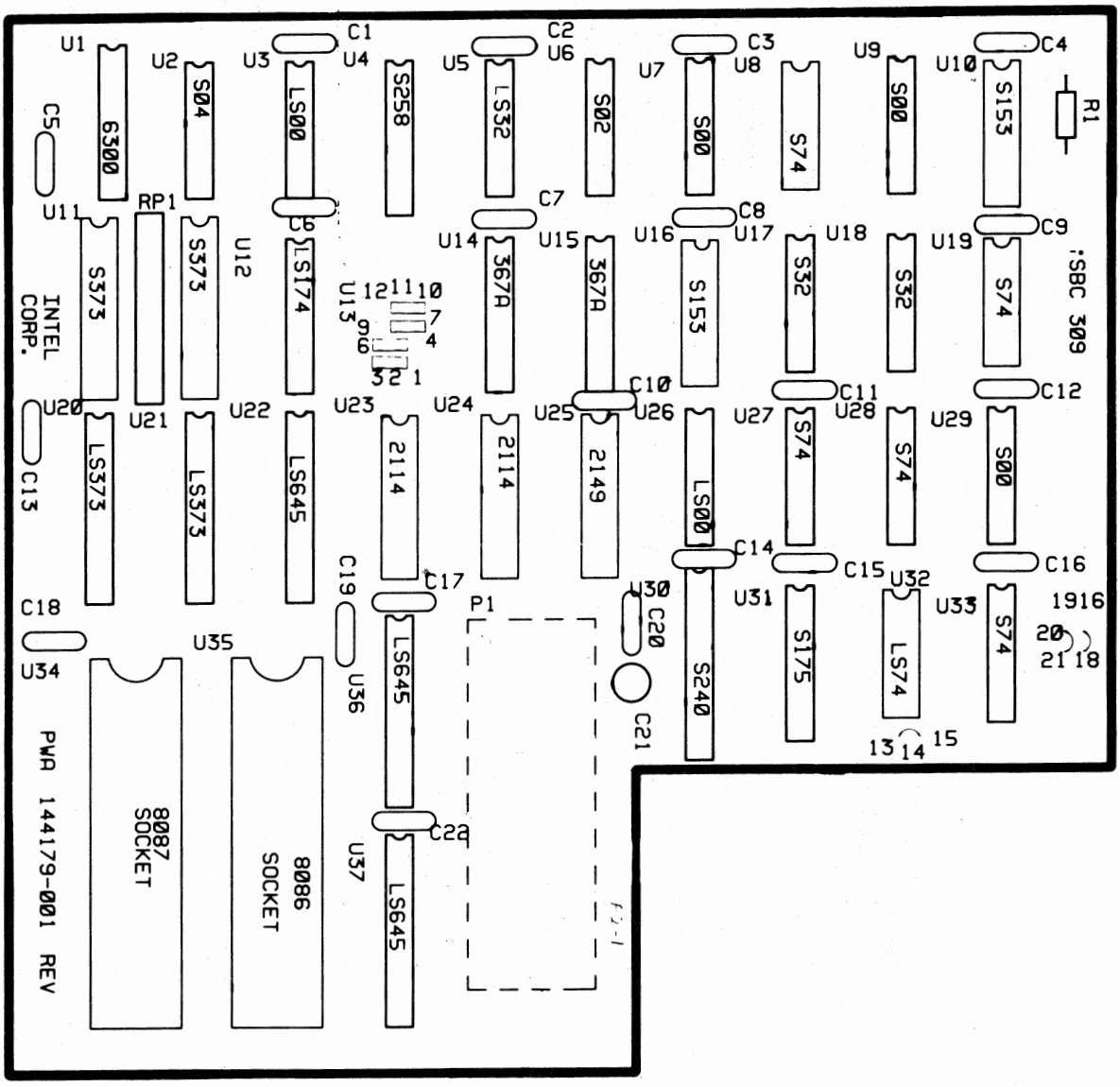


Figure 5-2. iSBC® 309 Board

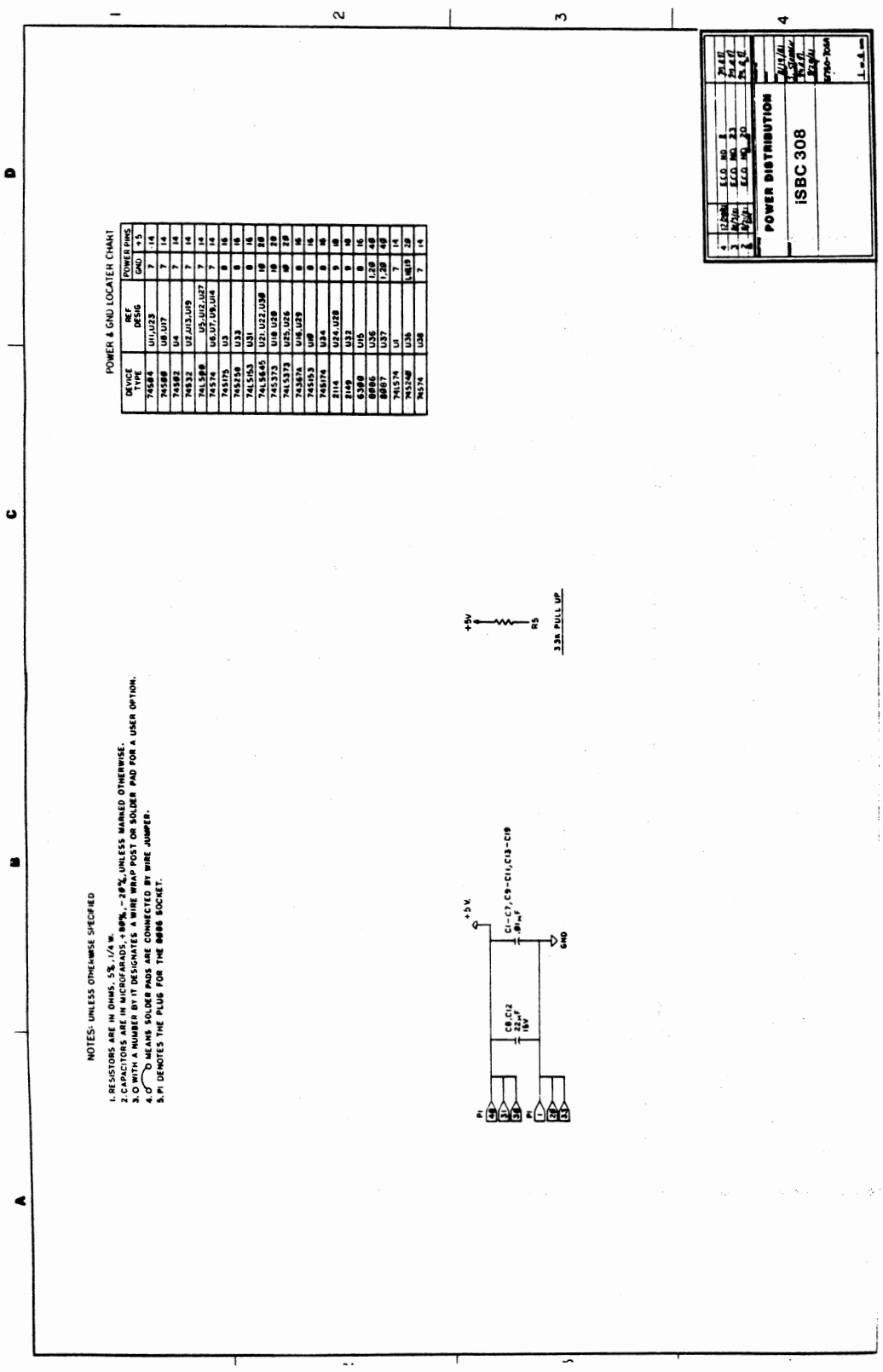

POWER & GND LOCATER CHART
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 5%, 1/4 W.
2. CAPACITORS ARE IN MICROFARADS, +80%, -20%, UNLESS MARKED OTHERWISE.
3. O WITH A NUMBER BY IT DESIGNATES A WIRE WRAP POST OR SOLDER PAD FOR A USER OPTION.
4. O MEANS SOLDER PADS ARE CONNECTED BY WIRE JUMPER.
5. P1 DENOTES THE PLUG FOR THE 8086 SOCKET.
+5V
R5
330 PULL UP
+5V
C1-C7, C9-C11, C13-C19
GND
C8, C12
22µF
16V
P1
POWER DISTRIBUTION
iSBC 308

Figure 5-3. iSBC® 308 Schematic Diagram (Sheet 1 of 4)

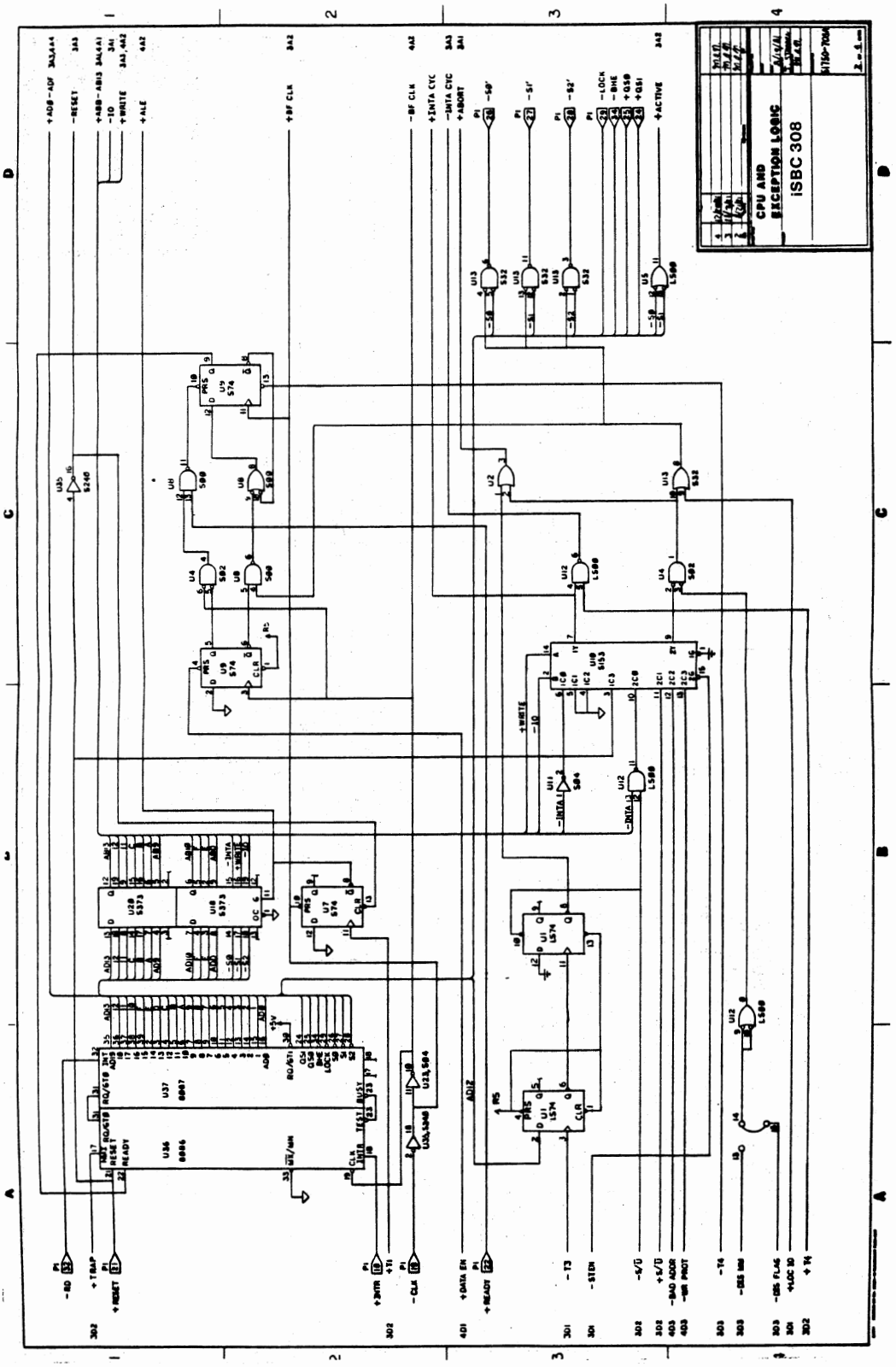


Figure 5-3. iSBC® 308 Schematic Diagram (Sheet 2 of 4)

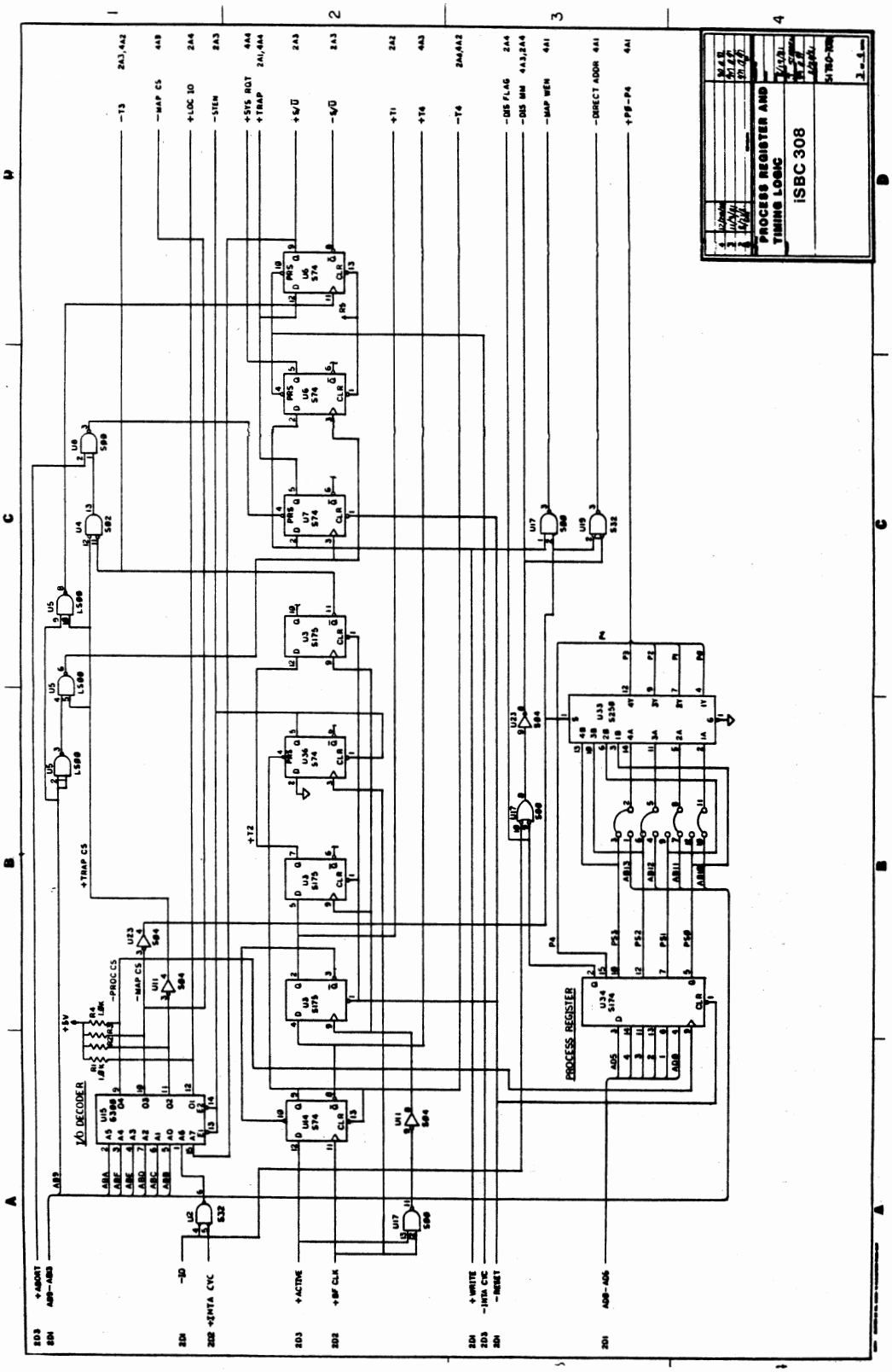


Figure 5-3. iSBC® 308 Schematic Diagram (Sheet 3 of 4)

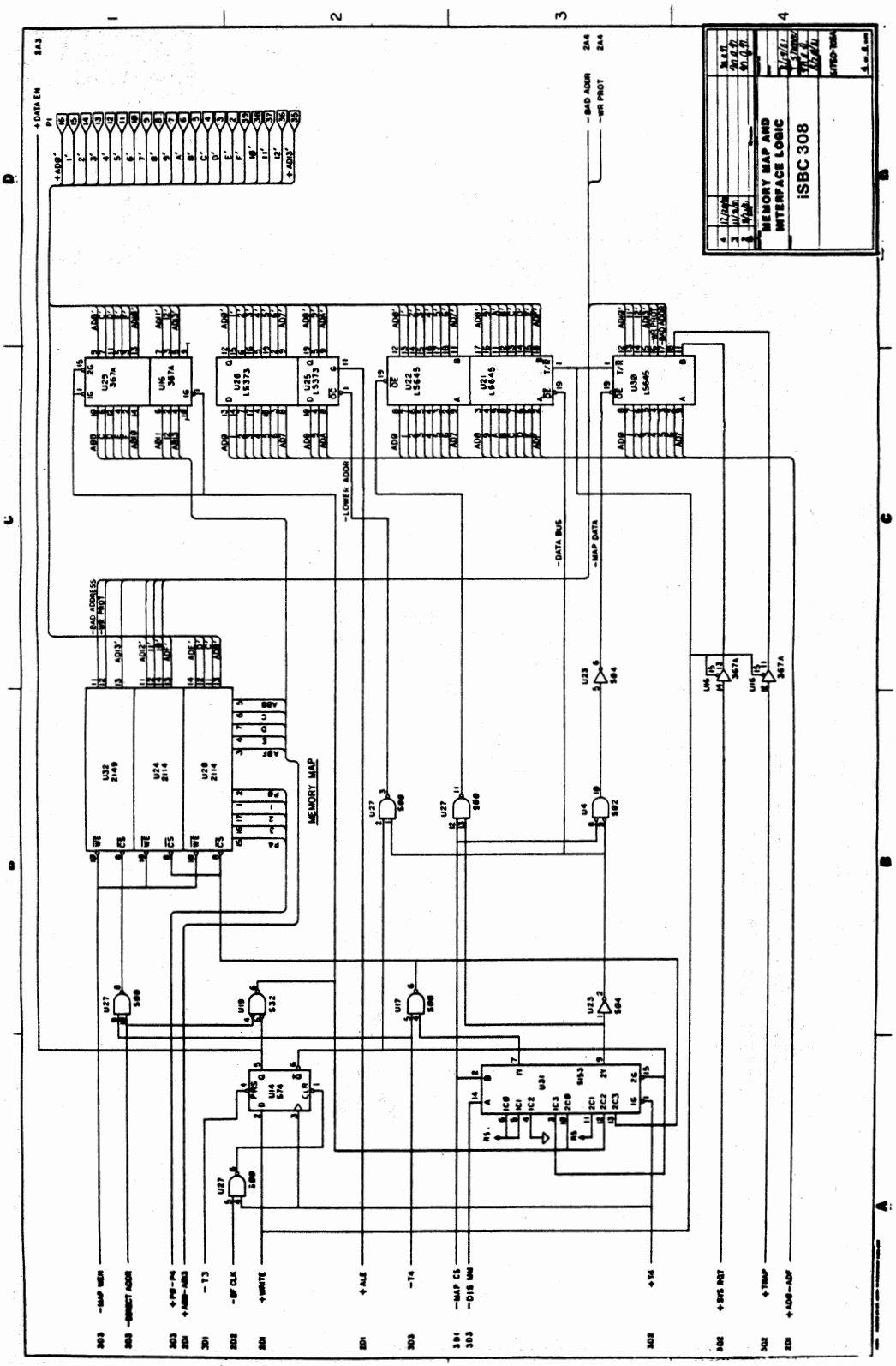


Figure 5-3. iSBC® 308 Schematic Diagram (Sheet 4 of 4)

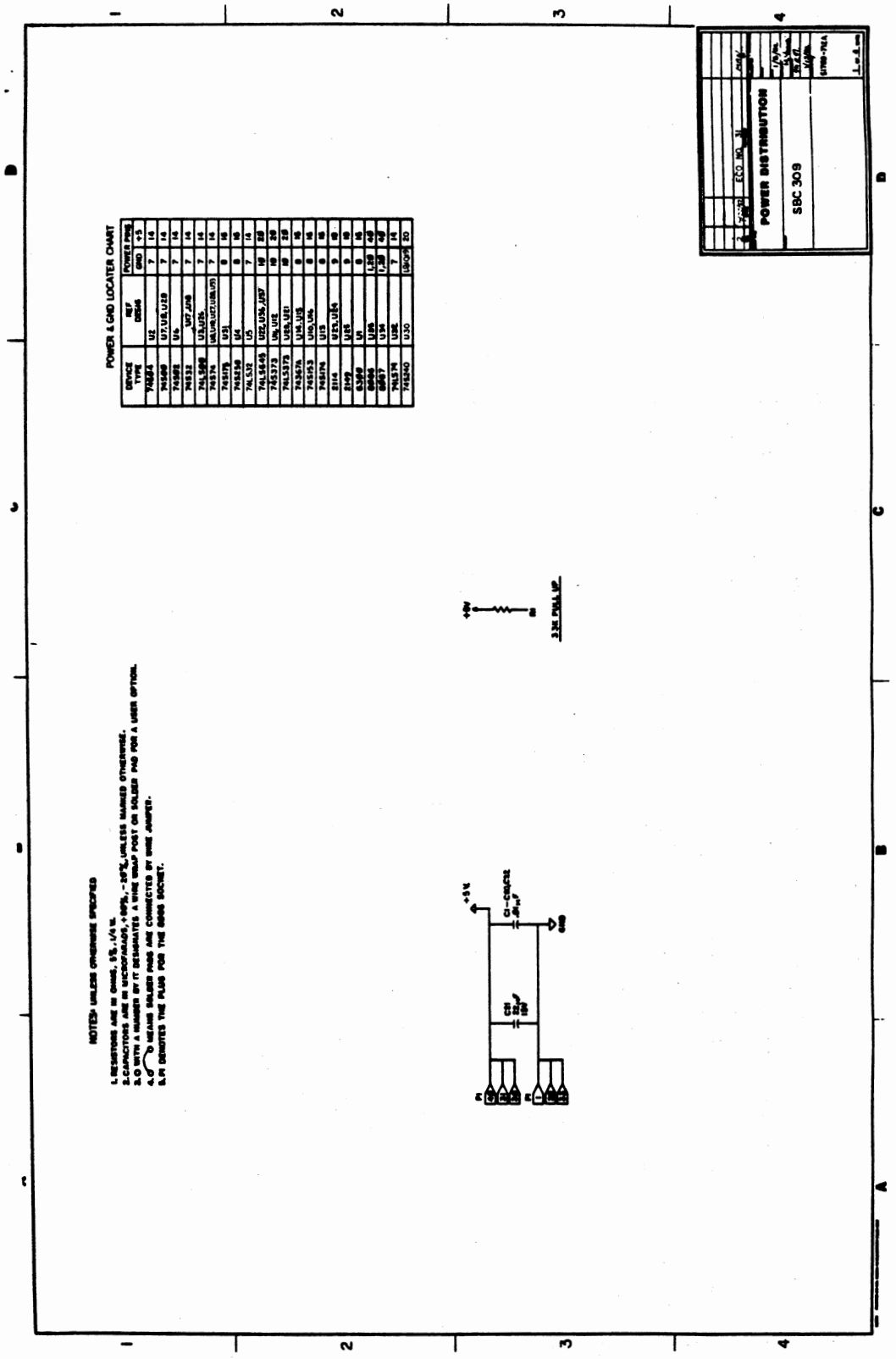


Figure 5-4. iSBC® 309 Schematic Diagram (Sheet 1 of 4)

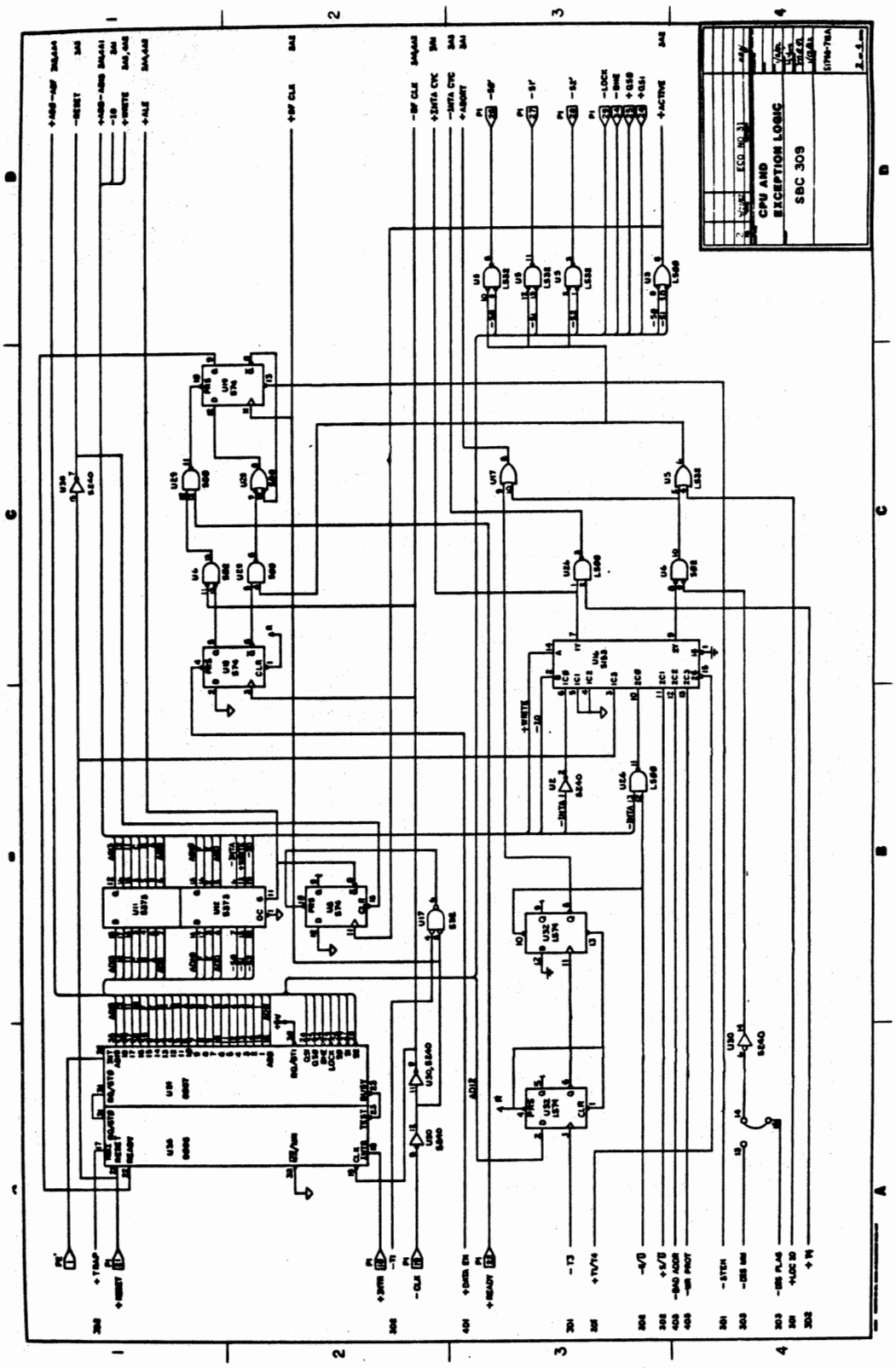


Figure 5-4. iSBC® 309 Schematic Diagram (Sheet 2 of 4)

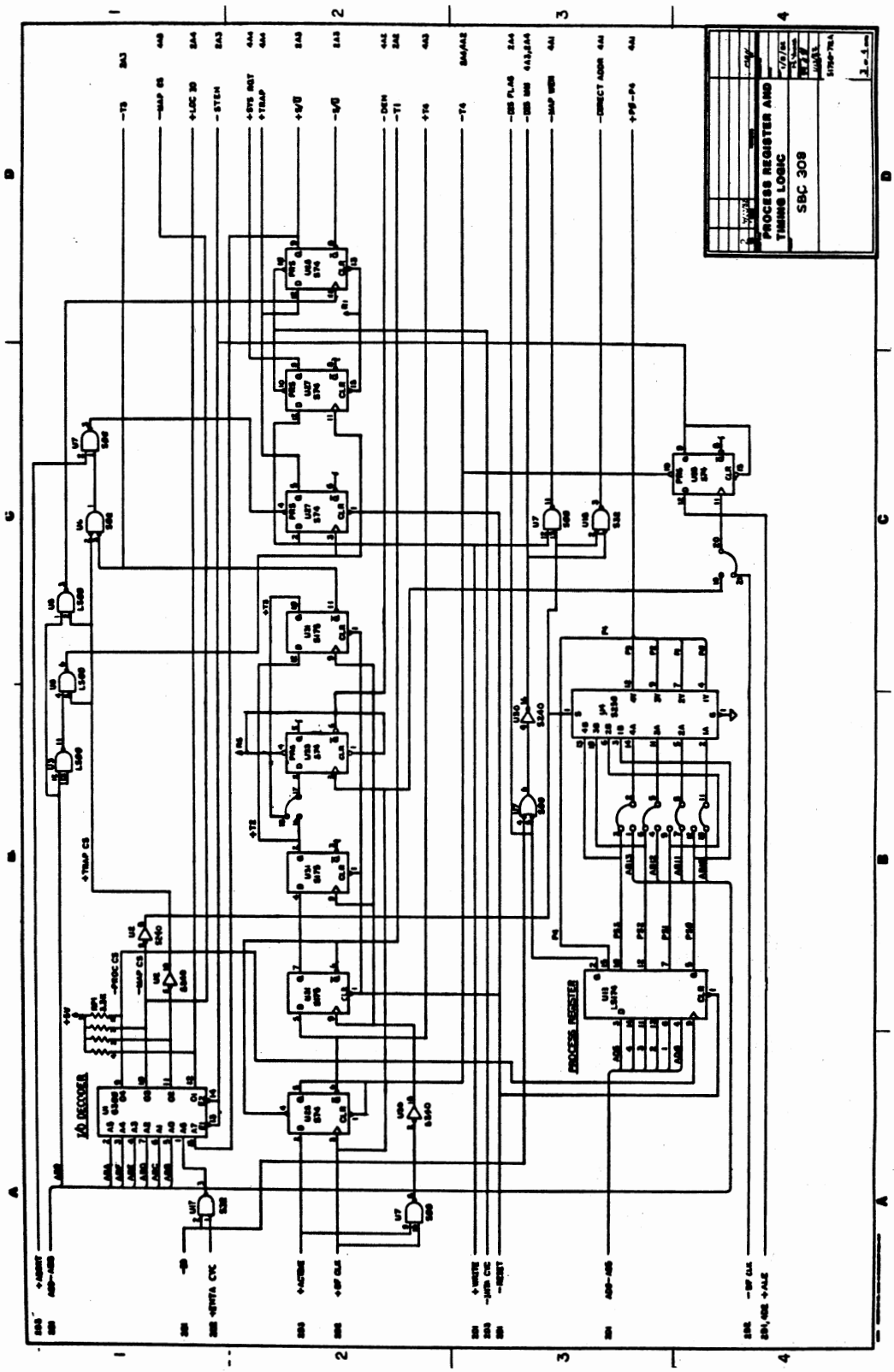


Figure 5-4. iSBC® 309 Schematic Diagram (Sheet 3 of 4)

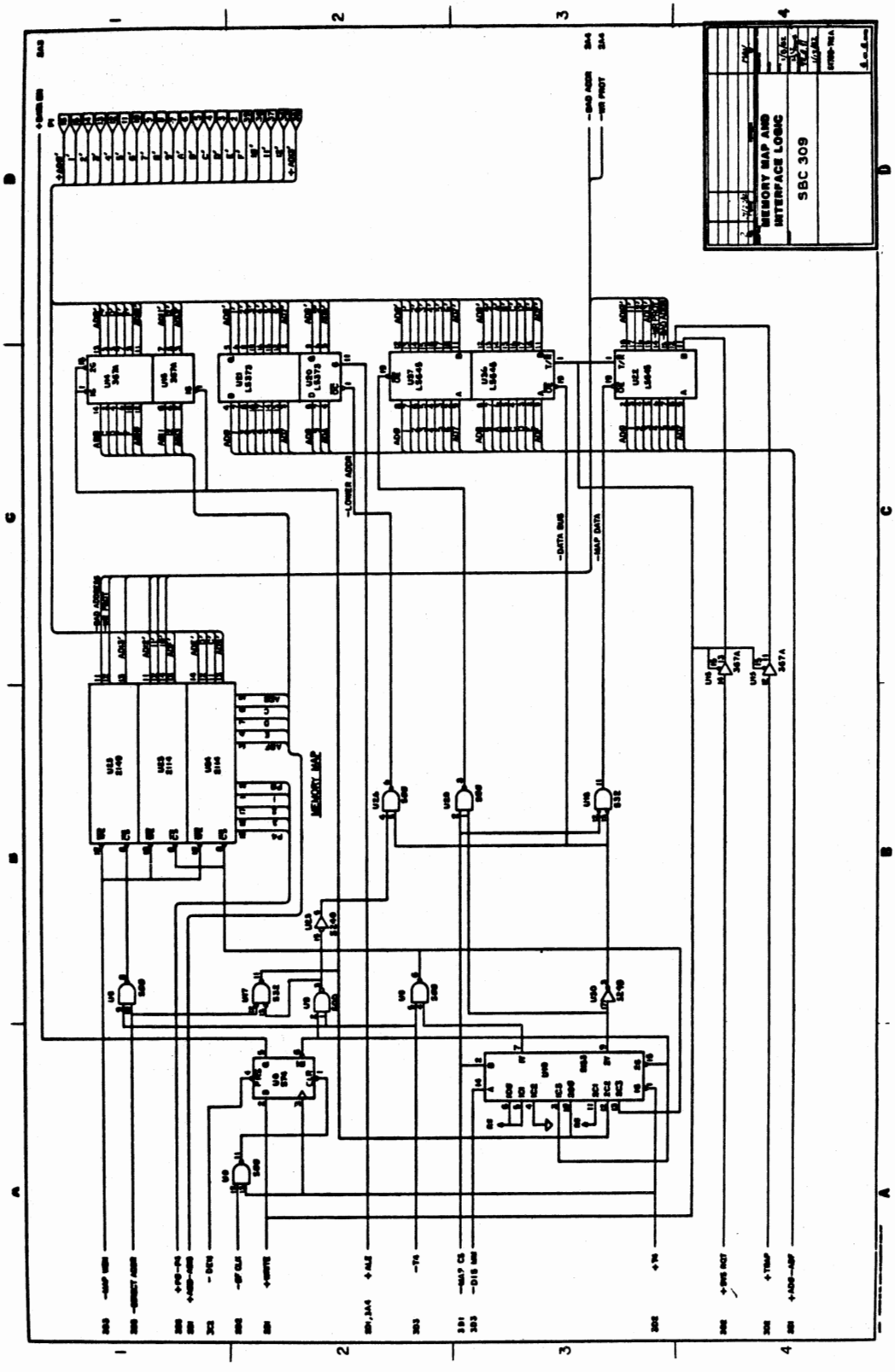


Figure 5-4. iSBC® 309 Schematic Diagram (Sheet 4 of 4)

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